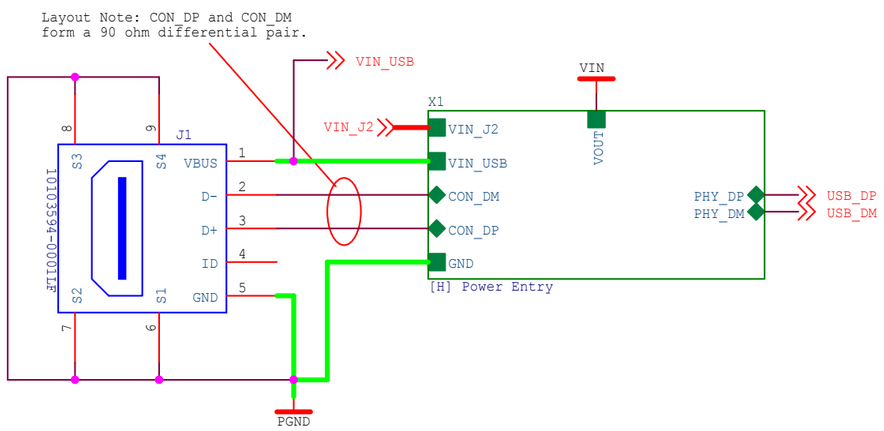
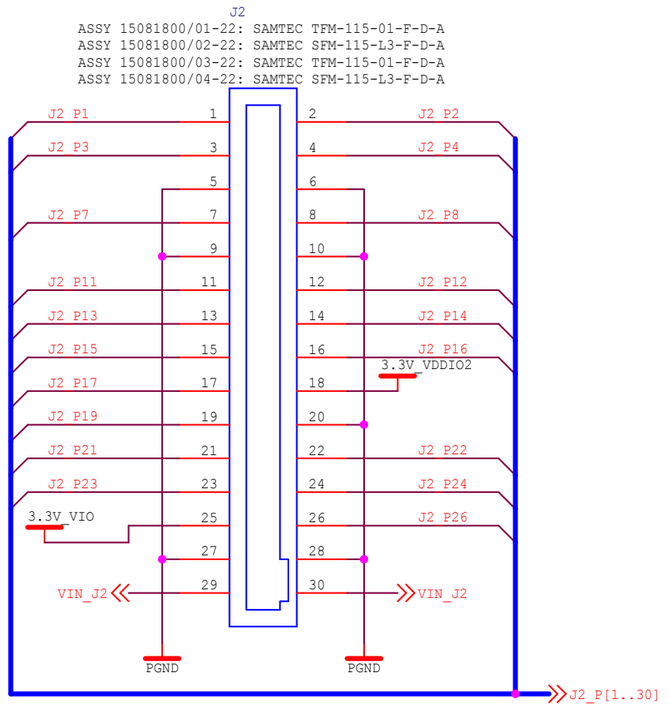
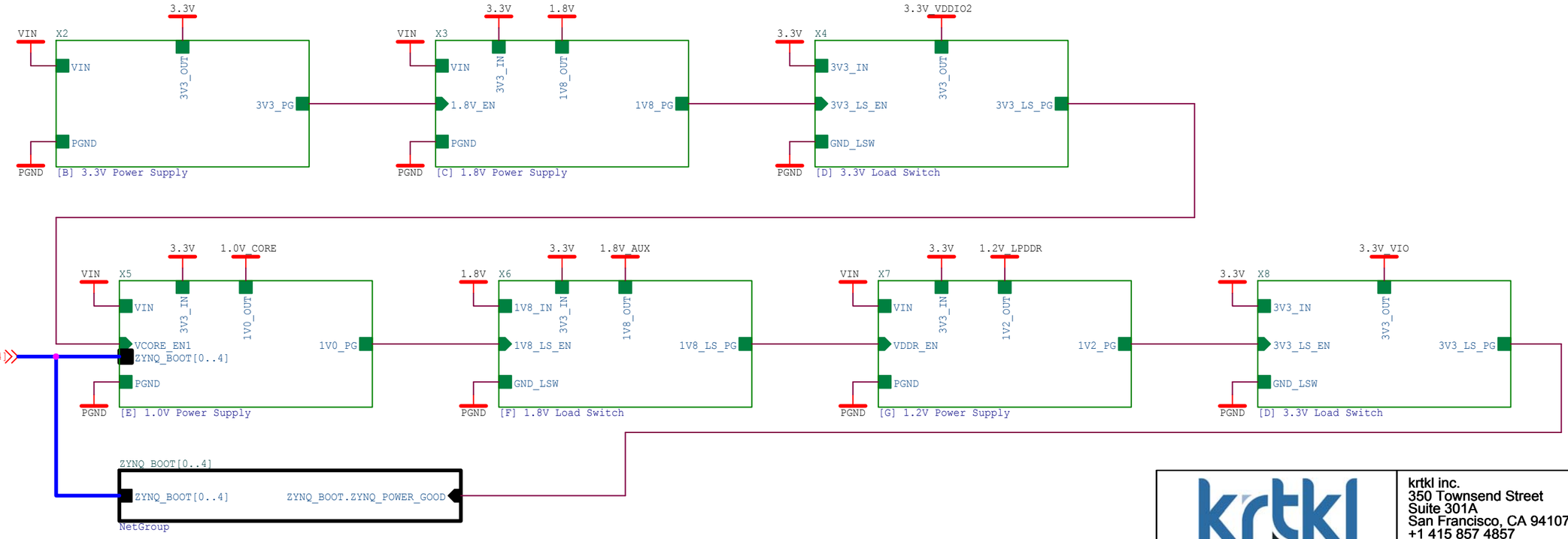
Rev.	Description	CO Number	Date	Approved By	Checked By
2	Alpha 2 Prototype	00001	09/01/2015	JJW	BEH
3	Beta 3 Prototype	00007	04/26/2016	JJW	BEH

Power/JTAG/SWD/BT Audio/I2C/DAC/ADC







Minimum Trace Ratings

6000mA	
4000mA	
2000mA	
1000mA	
200mA	

Minimum Plane Ratings

+VIN	4000mA
+3.3V	4000mA
+1.8V	2000mA
+3.3V_VDDIO2	4000mA
+1.0V_CORE	6000mA
+1.8V_AUX	2000mA
+1.2V_LPDDR	2000mA
+3.3V_VIO	4000mA

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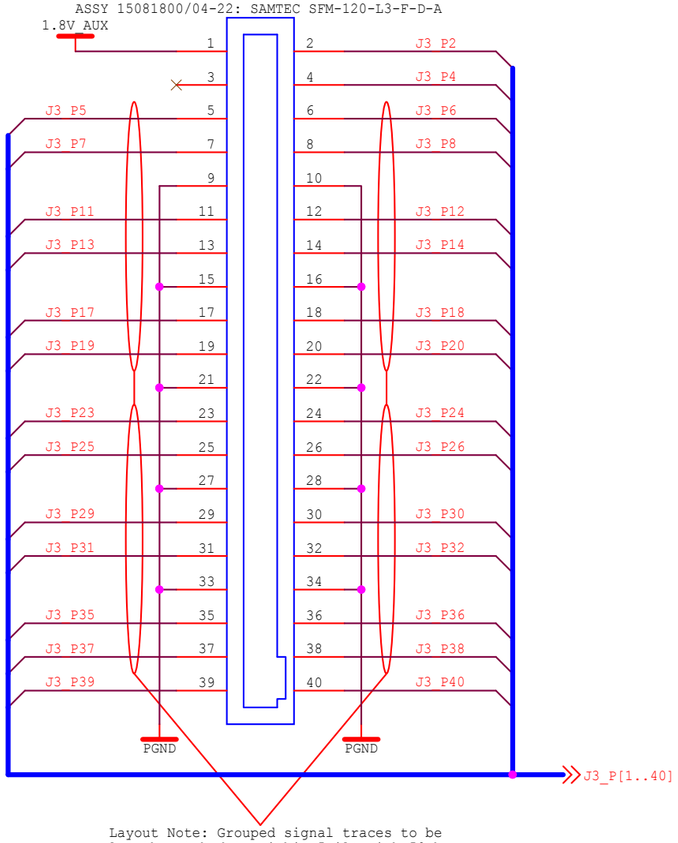
	NAME	DATE
DRAWN BY	J. Weatherbee	08/17/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 1 OF 30

CPU GPIO/USB ULPI/GigE RGMII/SPI/I2C/UART/CAN

J3

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A

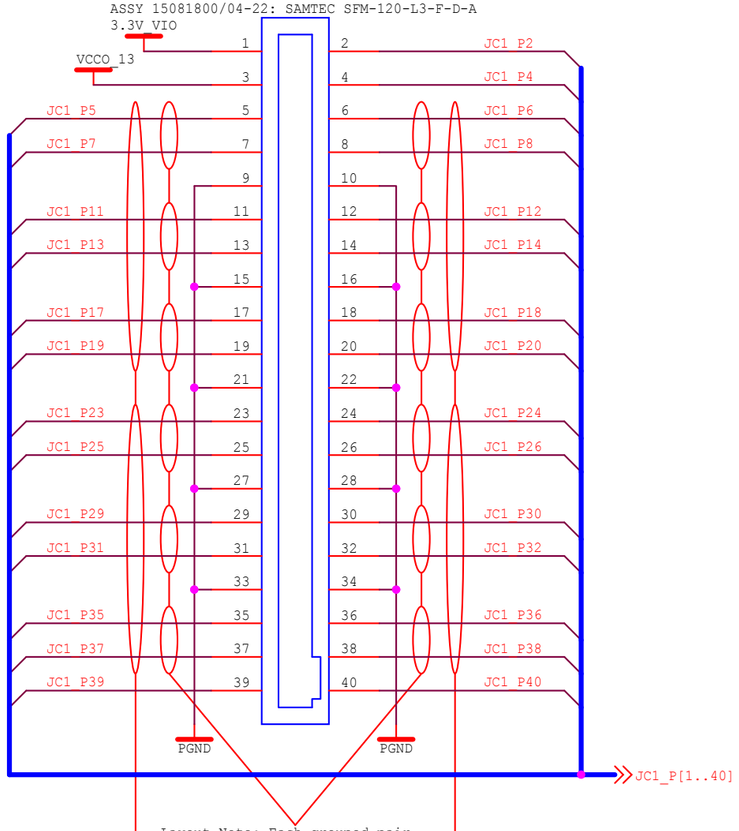


Layout Note: Grouped signal traces to be length matched to within 5mils with 50ohm single-ended characteristic impedance.

FPGA I/O

JC1

ASSY 15081800/01-22: NOT STUFFED
ASSY 15081800/02-22: NOT STUFFED
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A



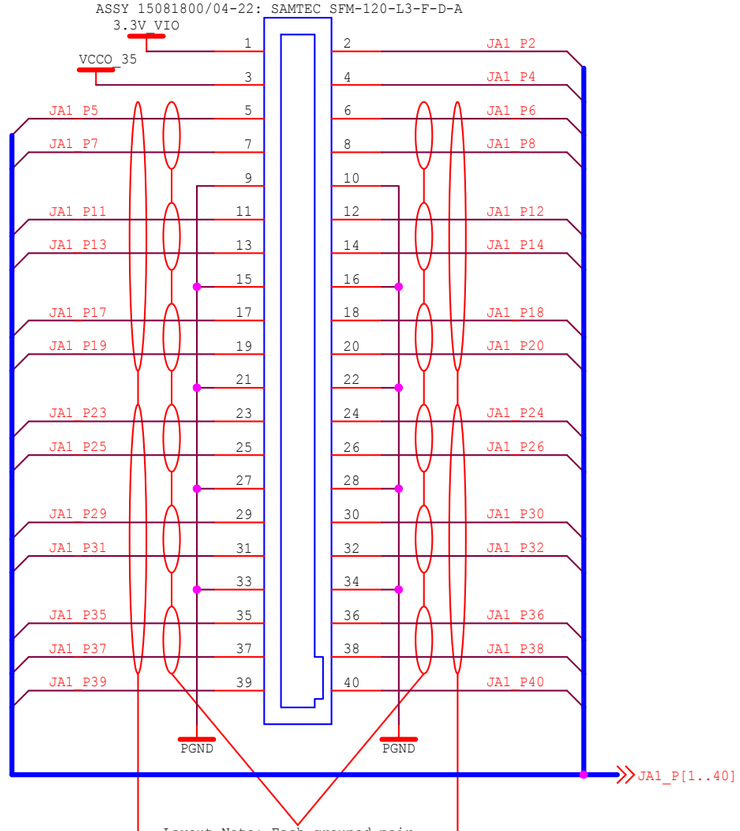
Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

FPGA I/O

JA1

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A



Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

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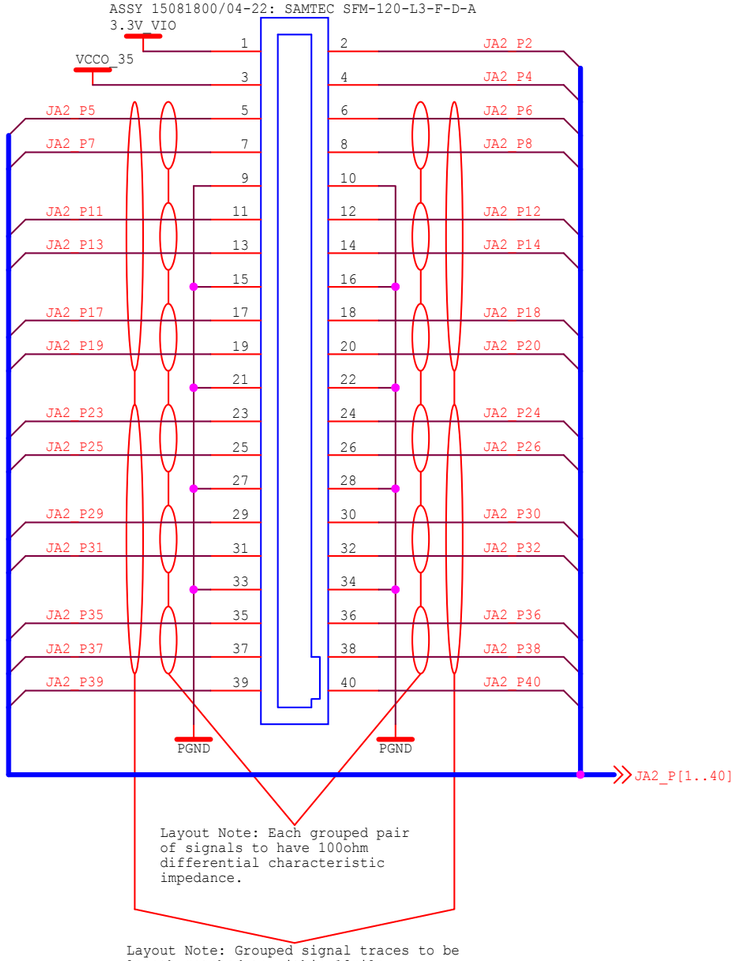
	NAME	DATE
DRAWN BY	J. Weatherbee	11/21/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 2 OF 30

FPGA I/O

JA2

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A
3.3V_VIO



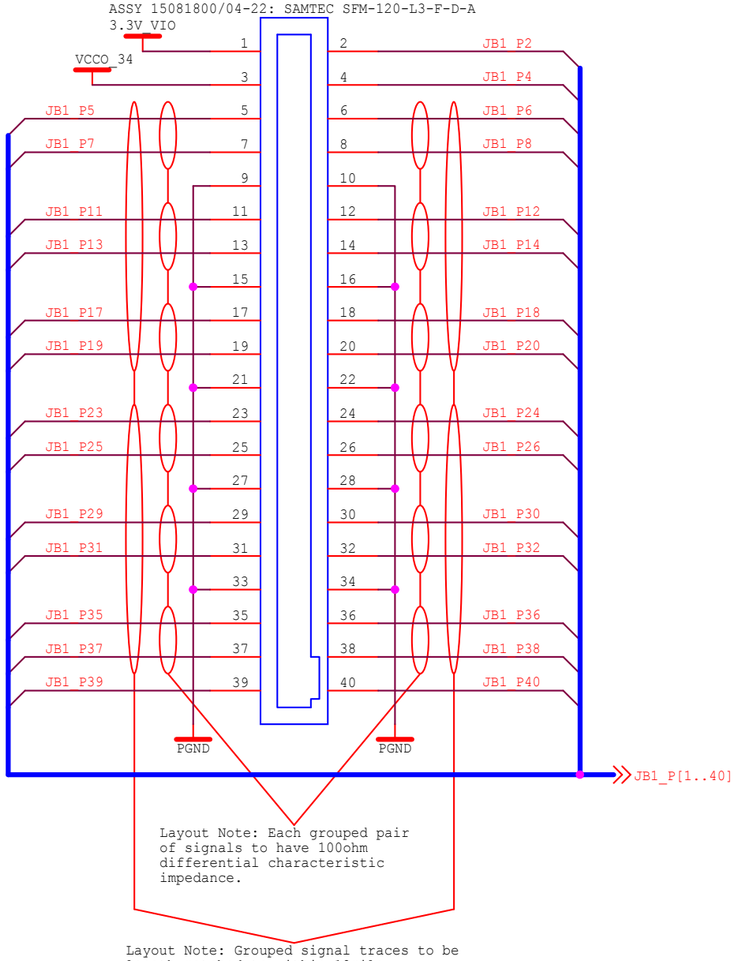
Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

FPGA I/O

JB1

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A
3.3V_VIO



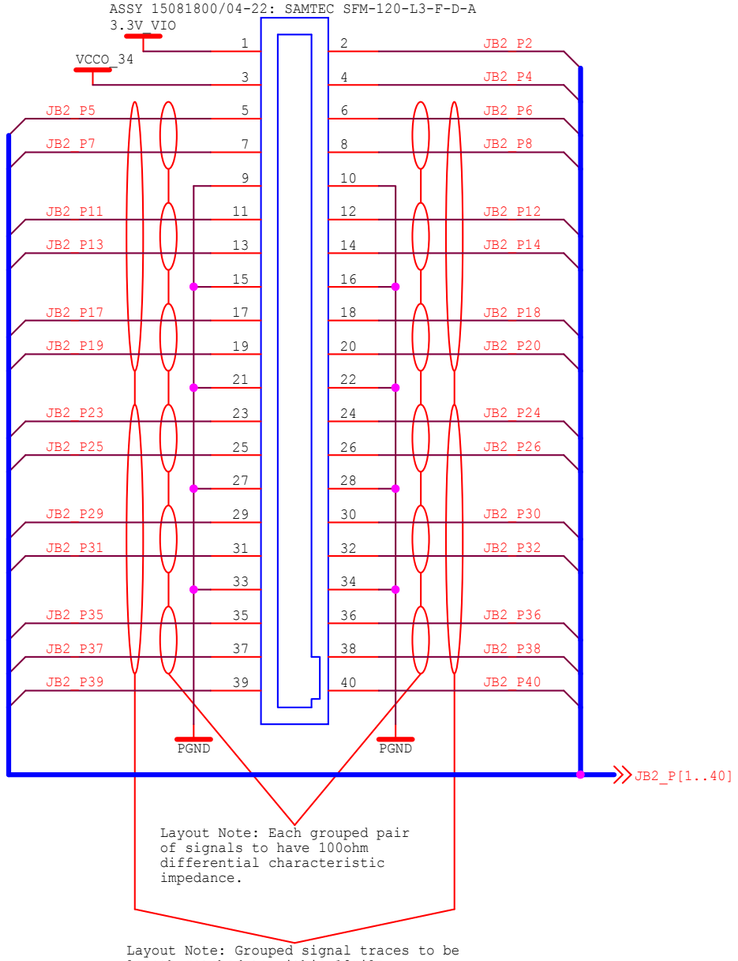
Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

FPGA I/O

JB2

ASSY 15081800/01-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/02-22: SAMTEC SFM-120-L3-F-D-A
ASSY 15081800/03-22: SAMTEC TFM-120-01-F-D-A
ASSY 15081800/04-22: SAMTEC SFM-120-L3-F-D-A
3.3V_VIO



Layout Note: Each grouped pair of signals to have 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

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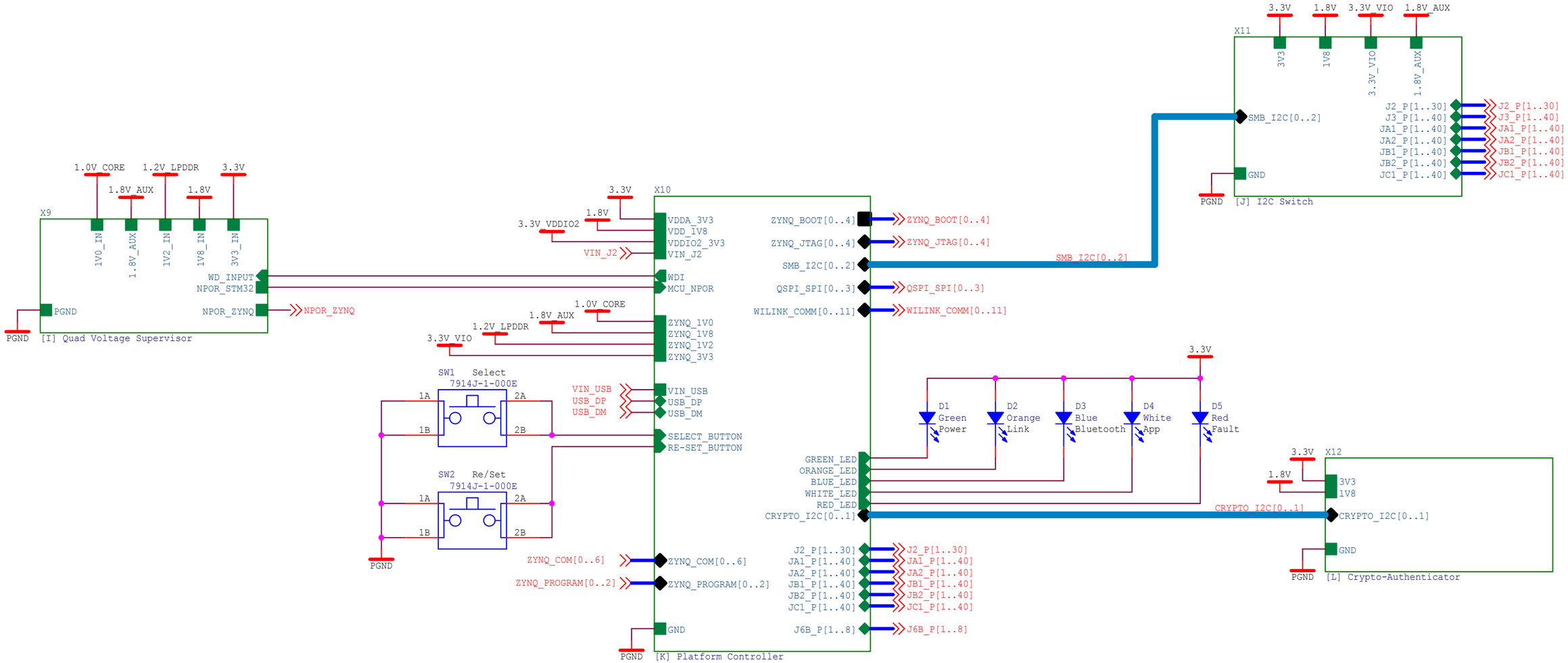
	NAME	DATE
DRAWN BY	J. Weatherbee	11/21/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 3 OF 30



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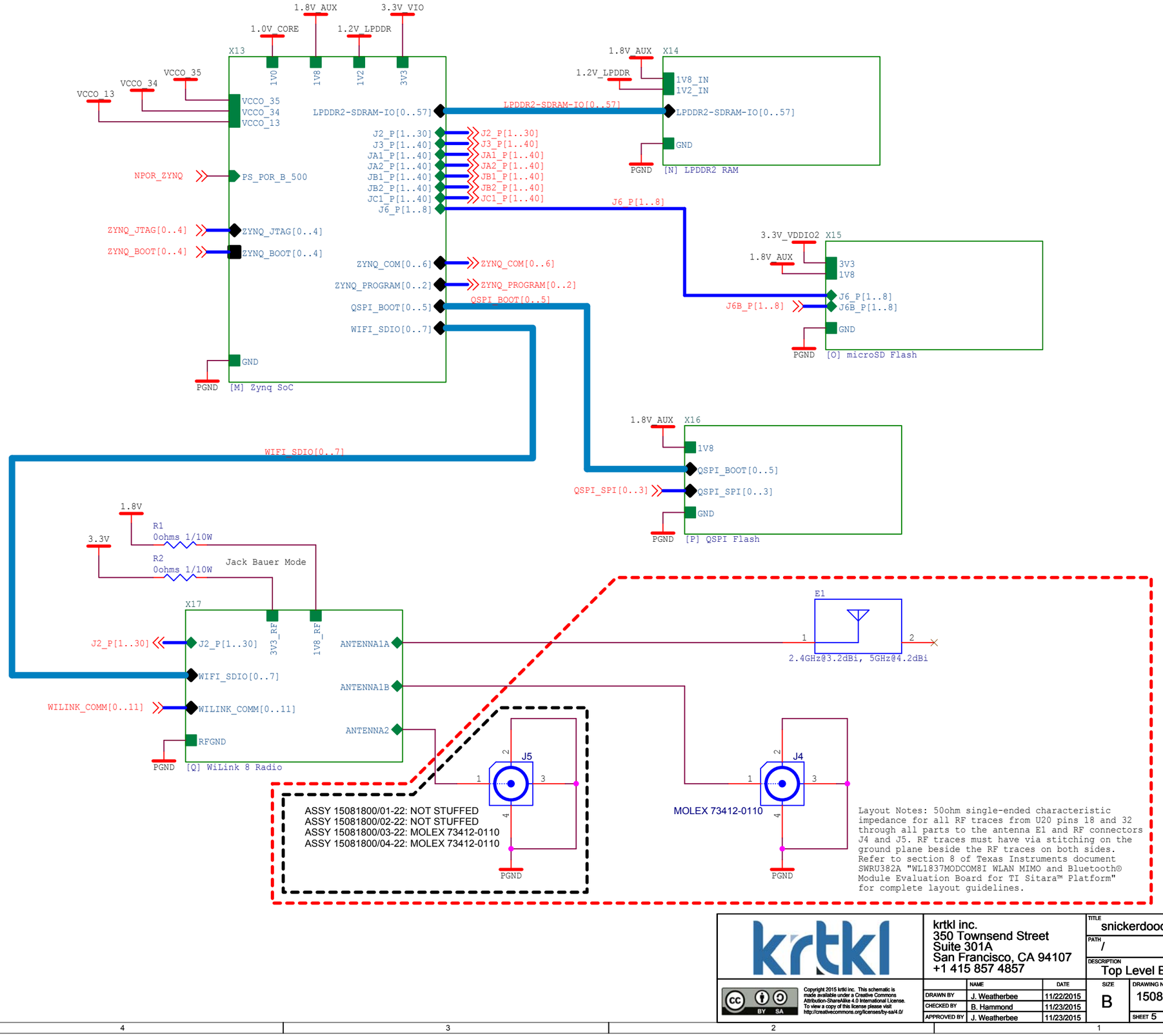
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 4 OF 30



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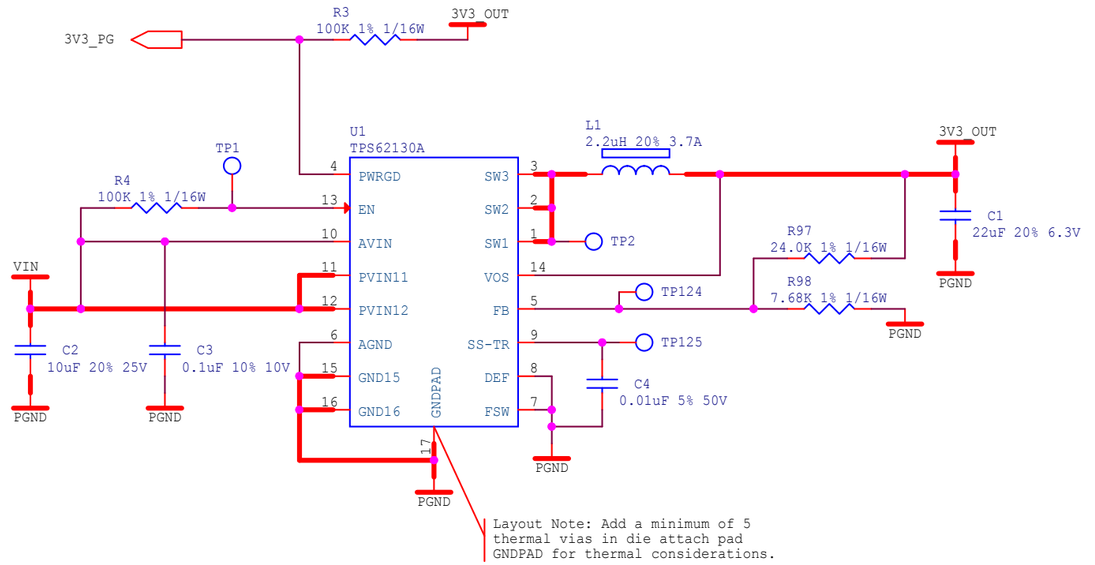
TITLE: snickerdoodle FPGA Module
PATH: /
DESCRIPTION: Top Level Block Diagram

	NAME	DATE
DRAWN BY	J. Weatherbee	11/22/2015
CHECKED BY	B. Hammond	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 5 OF 30



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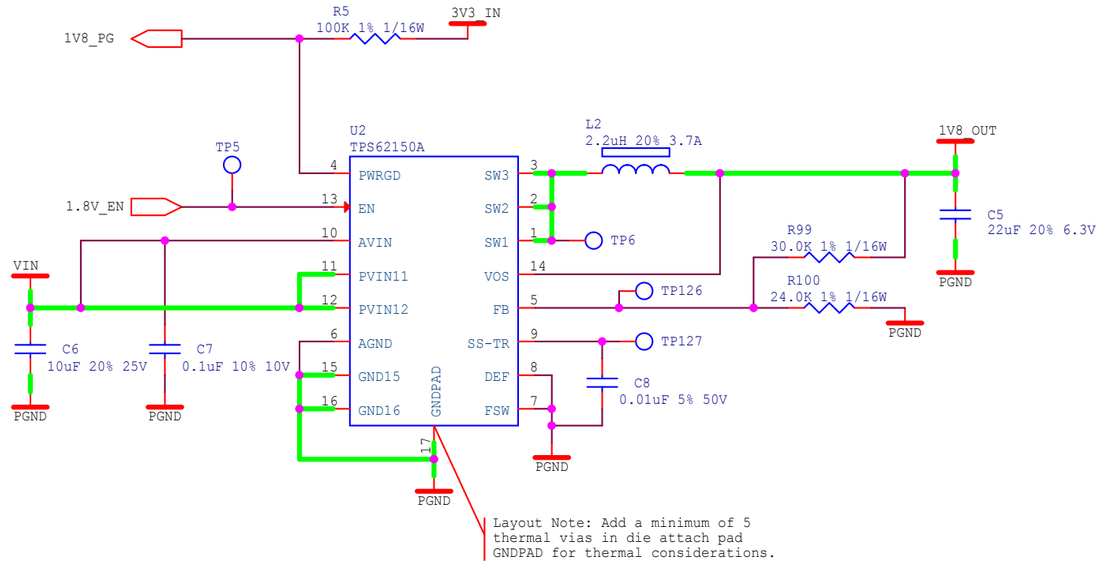
	NAME	DATE
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X2
DESCRIPTION: 3.3V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 6 OF 30



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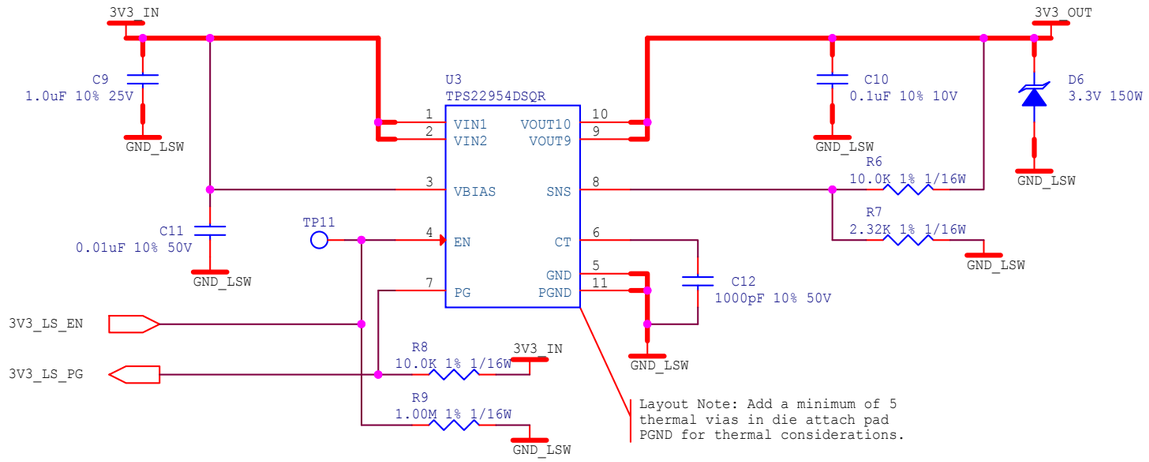
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X3
DESCRIPTION: 1.8V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 7 OF 30



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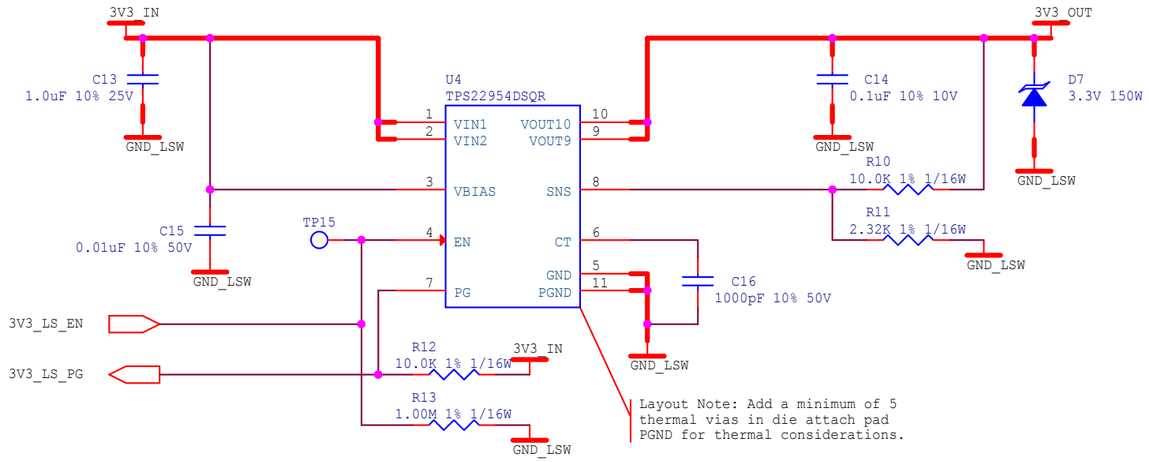
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X4
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 8 OF 30



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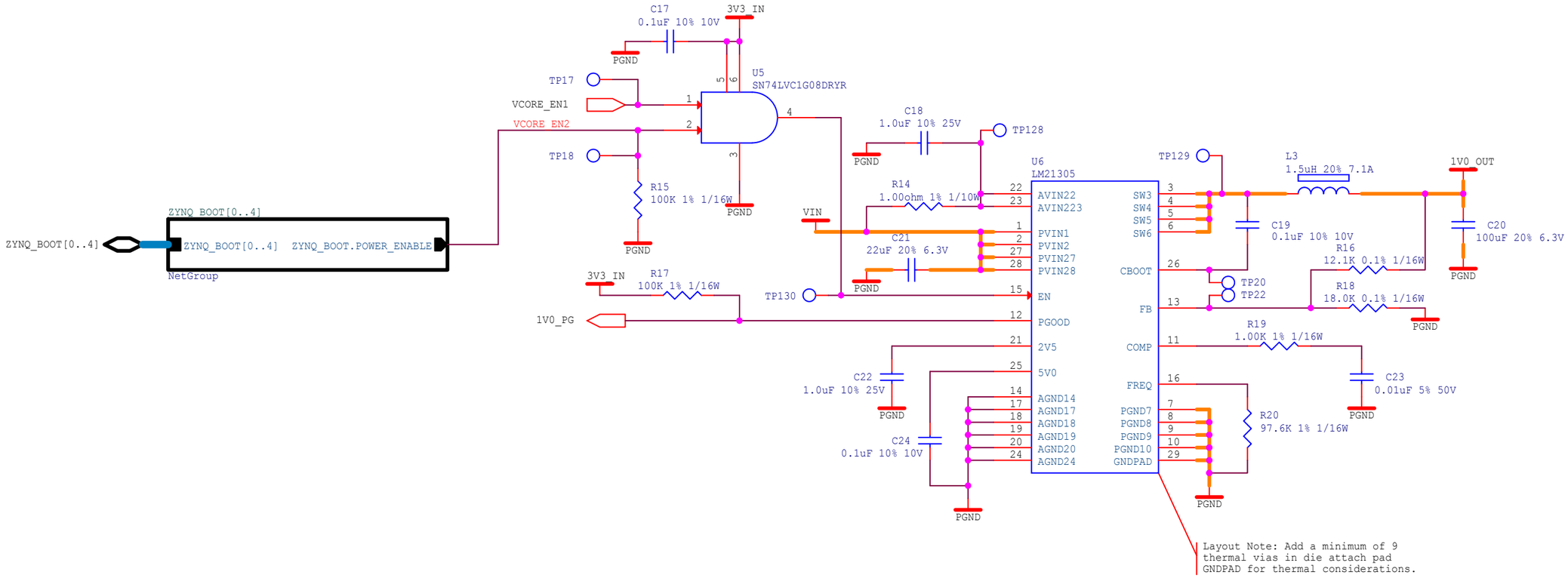
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X8
DESCRIPTION: 3.3V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 9 OF 30



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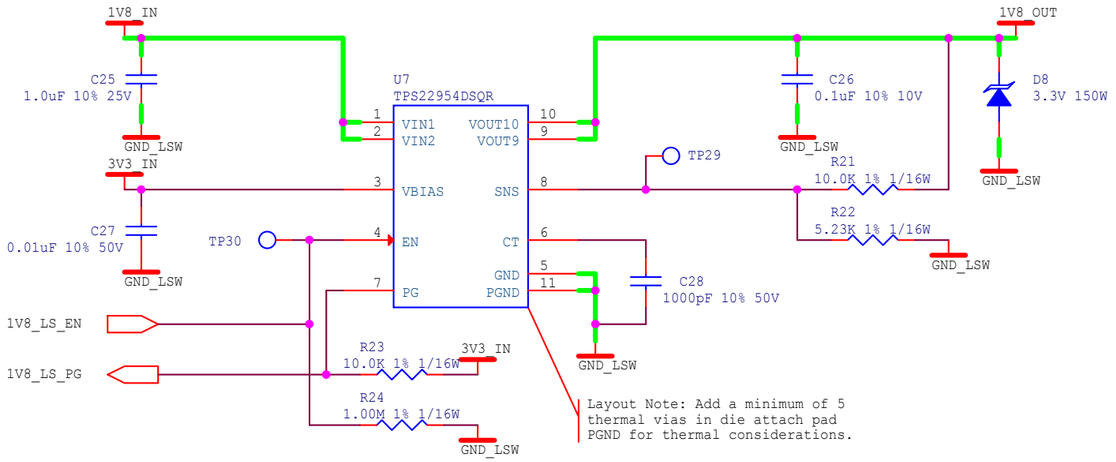
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X5
DESCRIPTION: 1.0V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 10 OF 30



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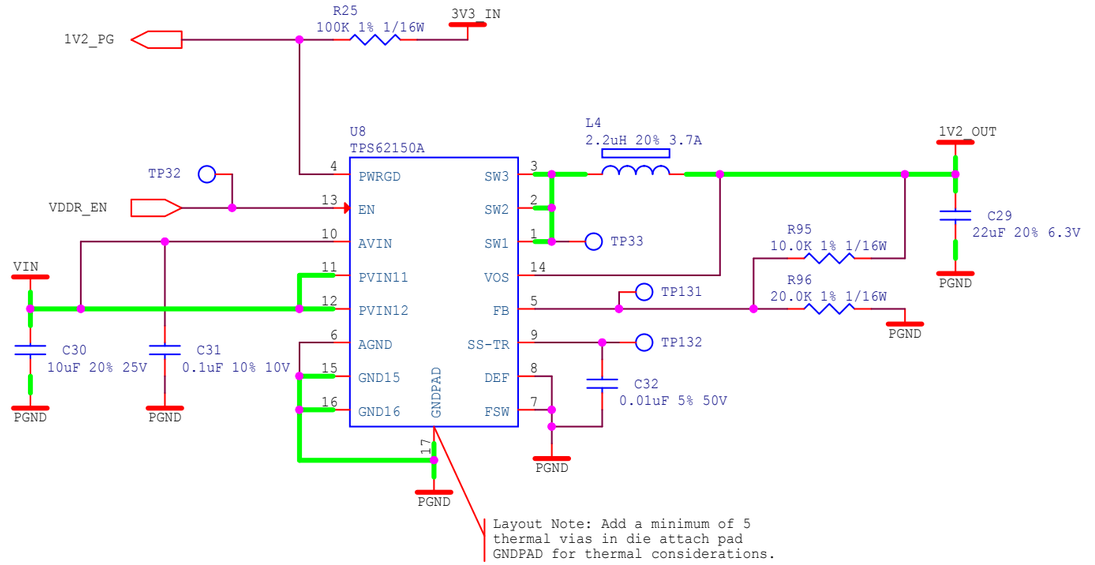
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X6
DESCRIPTION: 1.8V Load Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 11 OF 30



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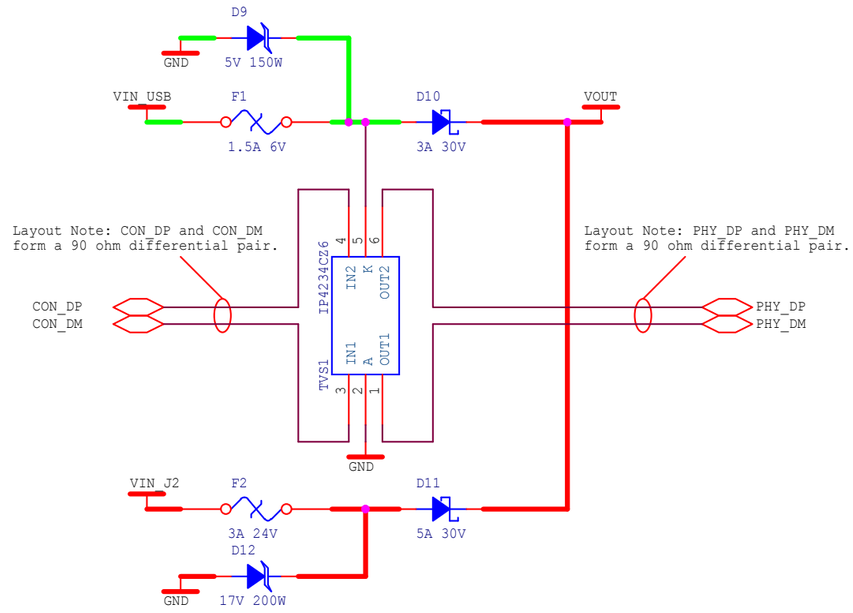
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X7
DESCRIPTION: 1.2V Power Supply
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 12 OF 30



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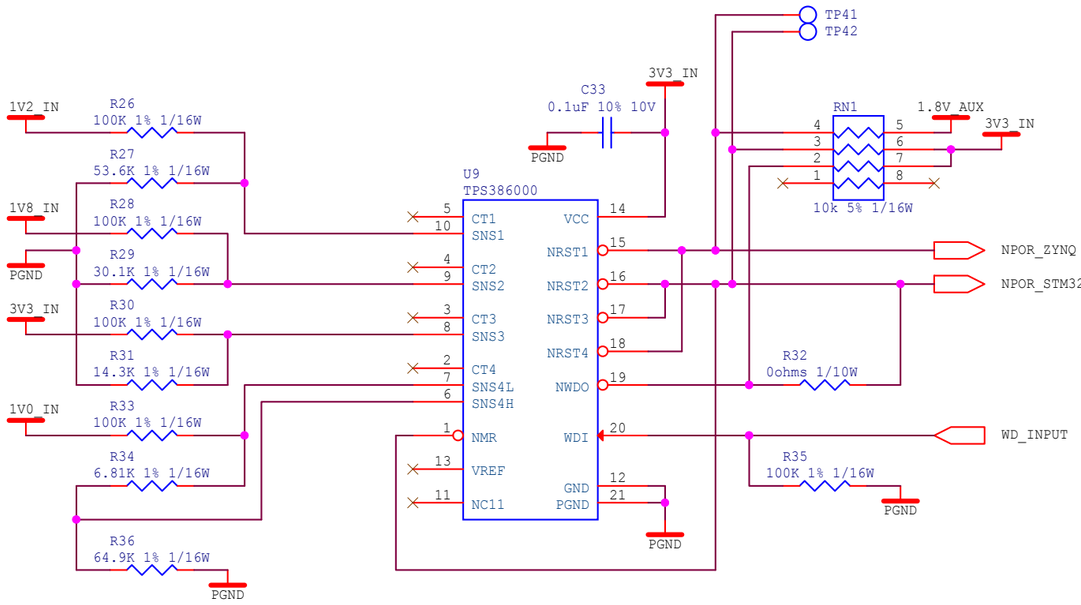
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X1
DESCRIPTION: Power Entry
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 13 OF 30



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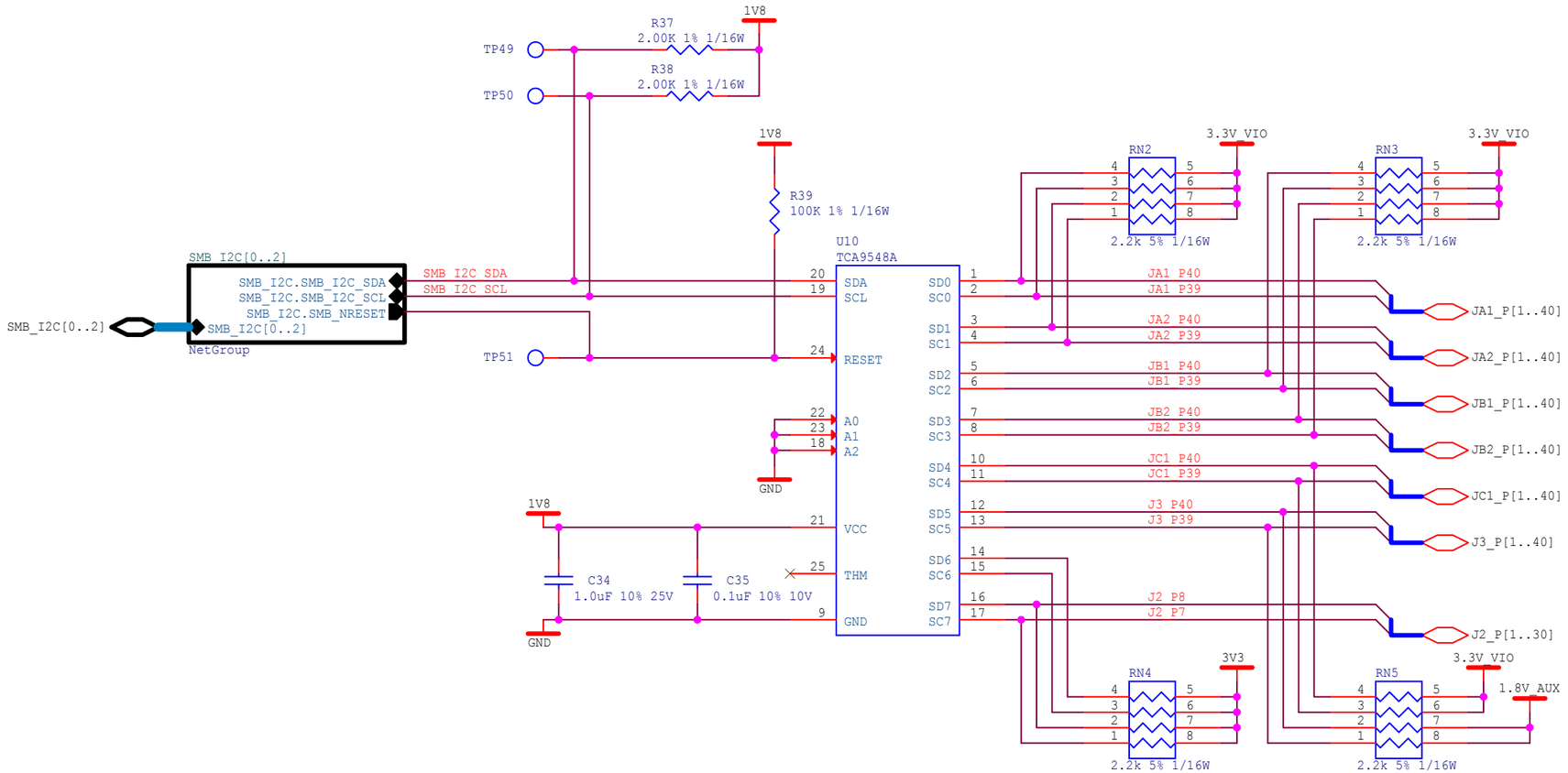
DRAWN BY	B. Hammond	11/21/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X9
DESCRIPTION: Quad Voltage Supervisor
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 14 OF 30



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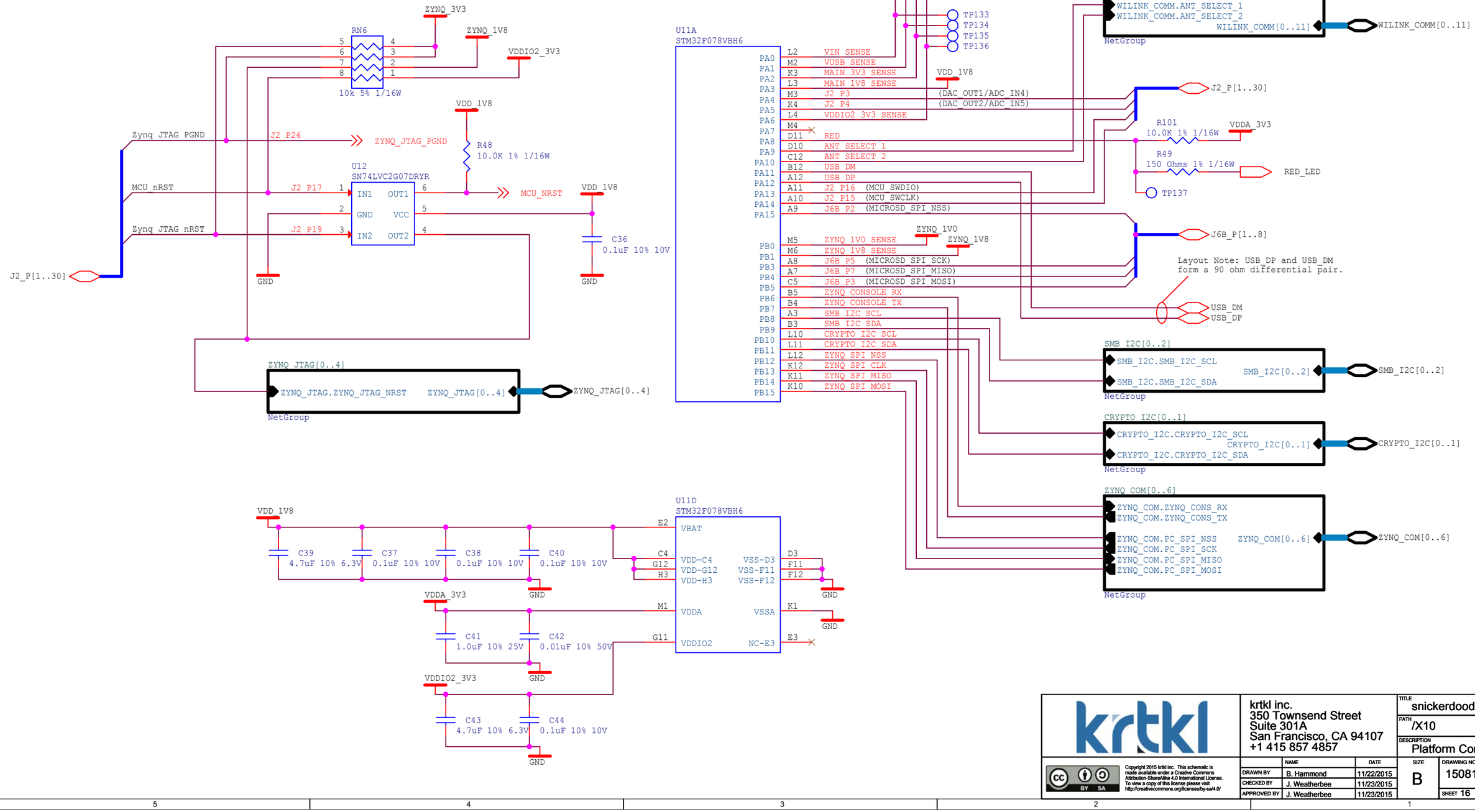
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X11
DESCRIPTION: I2C Switch
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 15 OF 30



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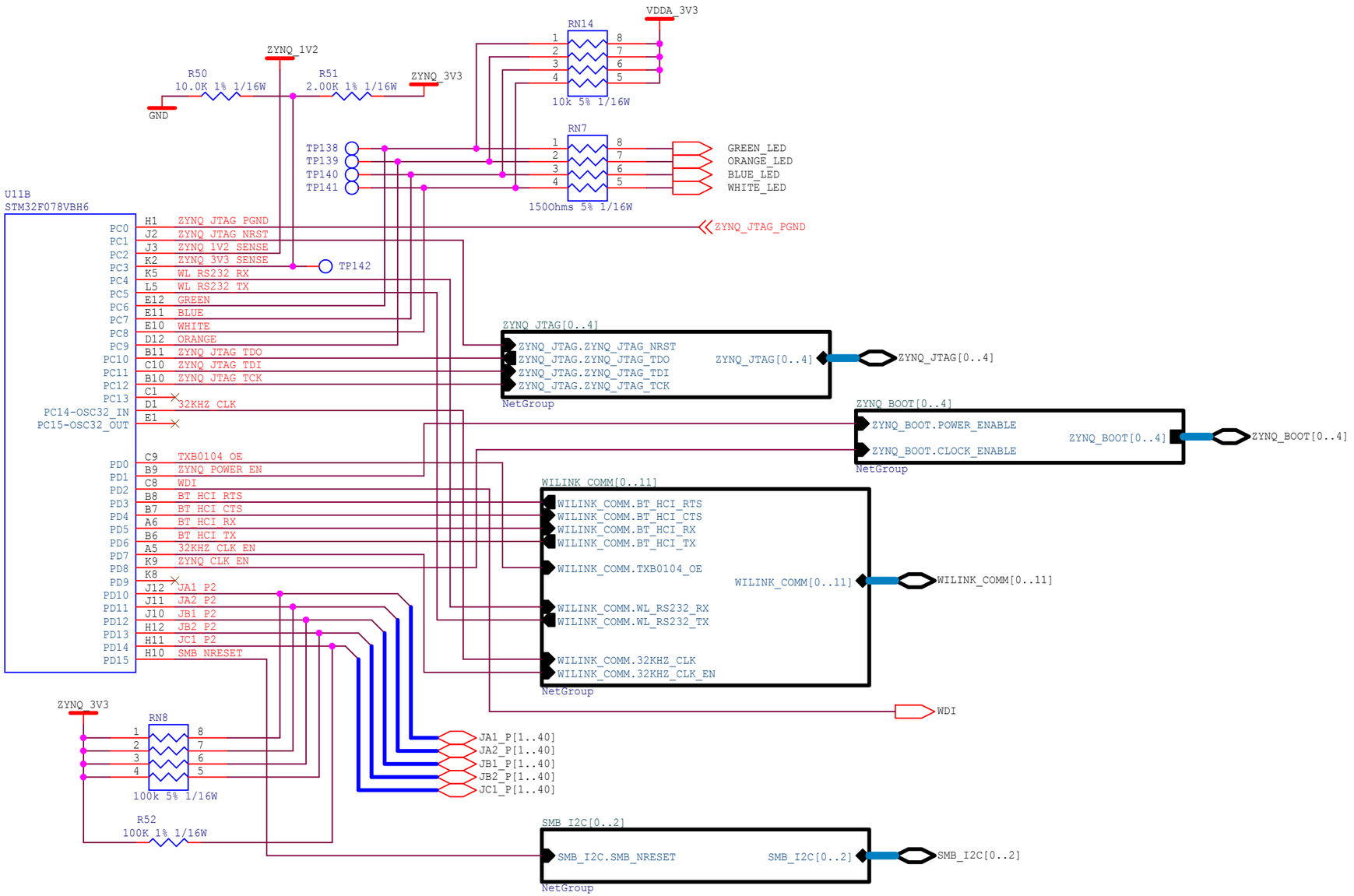
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 16 OF 30



krtkl inc. 350 Townsend Street Suite 301A San Francisco, CA 94107 +1 415 857 4857	TITLE: snickerdoodle FPGA Module PATH: /X10 DESCRIPTION: Platform Controller	
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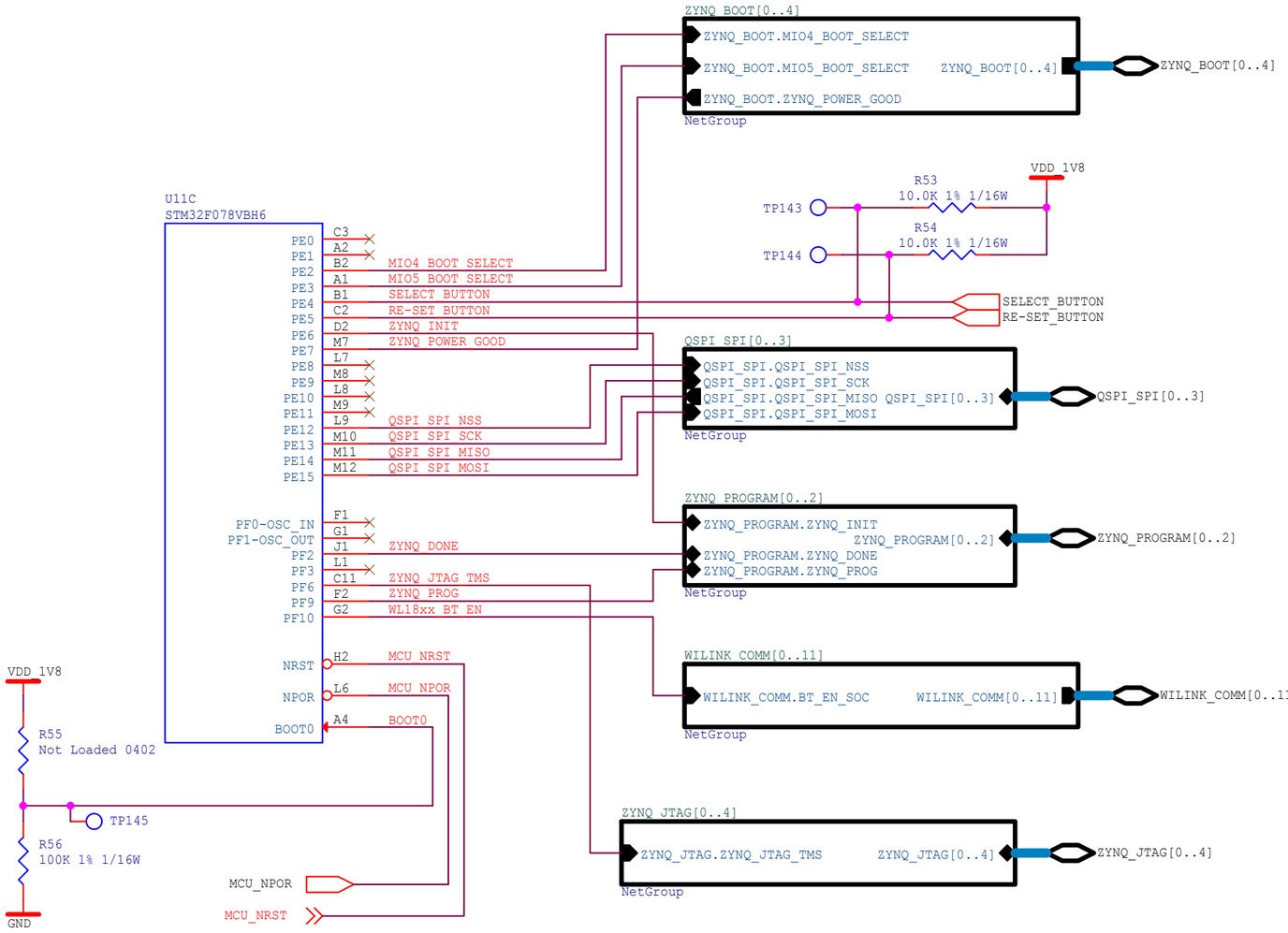

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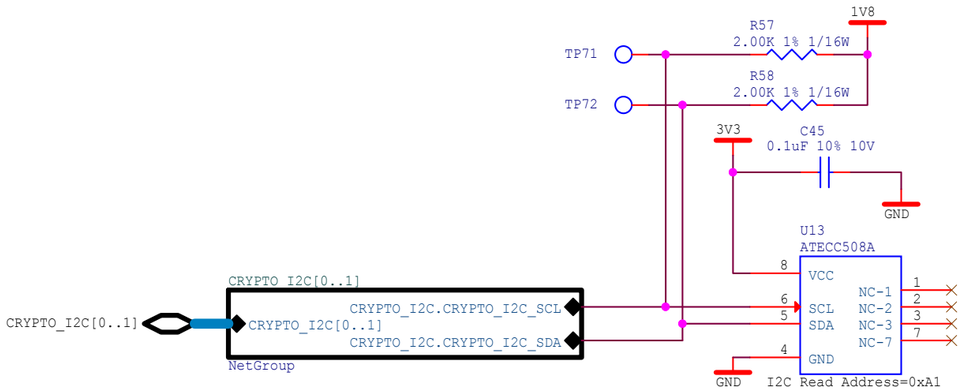
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X10
DESCRIPTION: Platform Controller
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 18 OF 30



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DRAWN BY	B. Hammond	11/22/2015
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APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X12
DESCRIPTION: Crypto-Authenticator
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 19 OF 30

U14H
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

DIGITAL GND

A8	GND-A8	GND-L8	L8
A18	GND-A18	GND-L12	L12
B1	GND-B1	GND-L18	L18
B11	GND-B11	GND-M1	M1
C4	GND-C4	GND-M7	M7
C9	GND-C9	GND-M11	M11
C14	GND-C14	GND-M13	M13
D17	GND-D17	GND-N4	N4
E10	GND-E10	GND-N8	N8
E20	GND-E20	GND-N10	N10
F3	GND-F3	GND-N12	N12
F7	GND-F7	GND-N14	N14
G10	GND-G10	GND-P7	P7
G12	GND-G12	GND-P9	P9
G16	GND-G16	GND-P11	P11
H7	GND-H7	GND-P13	P13
H9	GND-H9	GND-P17	P17
H11	GND-H11	GND-R8	R8
H13	GND-H13	GND-R12	R12
H19	GND-H19	GND-R20	R20
J2	GND-J2	GND-T3	T3
J8	GND-J8	GND-T7	T7
J12	GND-J12	GND-T13	T13
K5	GND-K5	GND-U6	U6
K7	GND-K7	GND-U16	U16
K11	GND-K11	GND-V9	V9
K13	GND-K13	GND-V19	V19
K15	GND-K15	GND-W2	W2
		GND-W12	W12
		GND-Y5	Y5
		GND-Y15	Y15

GND

U14J
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

I/O POWER

3V3 — C46 47uF 20% 6.3V — GND

	VCCO_0	VCCO_DDR_502-A3	A3
		VCCO_DDR_502-D2	D2
		VCCO_DDR_502-E5	E5
		VCCO_DDR_502-G1	G1
		VCCO_DDR_502-H4	H4
T8	VCCO_13-T8	VCCO_DDR_502-L3	L3
U11	VCCO_13-U11	VCCO_DDR_502-P2	P2
W7	VCCO_13-W7	VCCO_DDR_502-R5	R5
Y10	VCCO_13-Y10	VCCO_DDR_502-U1	U1
		VCCO_DDR_502-V4	V4
N19	VCCO_34-N19		
R15	VCCO_34-R15		
T18	VCCO_34-T18	VCCO_MIO0_500-B6	B6
V14	VCCO_34-V14	VCCO_MIO0_500-D7	D7
W17	VCCO_34-W17		
Y20	VCCO_34-Y20		
		VCCO_MIO1_501-A13	A13
		VCCO_MIO1_501-B16	B16
C19	VCCO_35-C19	VCCO_MIO1_501-D12	D12
F18	VCCO_35-F18	VCCO_MIO1_501-E15	E15
H14	VCCO_35-H14		
J17	VCCO_35-J17		
K20	VCCO_35-K20	PS_DDR_VREF0_502	H6
M16	VCCO_35-M16	PS_DDR_VREF1_502	P6

1V2 — R59 80.6 ohm 1% 1/16W
R60 80.6 ohm 1% 1/16W
C47 0.47uF 10% 6.3V
GND

U14I
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

CORE POWER

	VCCINT-G13	G13
	VCCINT-H12	H12
	VCCINT-J13	J13
	VCCINT-K12	K12
	VCCINT-L13	L13
	VCCINT-M12	M12
	VCCINT-N13	N13
	VCCINT-P12	P12
	VCCINT-R13	R13
	VCCAUX-J11	J11
	VCCAUX-L11	L11
	VCCAUX-N11	N11
	VCCAUX-N9	N9
	VCCAUX-P10	P10
	VCCAUX-R9	R9
	VCCPAUX-F8	F8
	VCCPAUX-G9	G9
	VCCPAUX-H8	H8
	VCCPAUX-K8	K8
	VCCPAUX-M8	M8
	VCCBRAM-G11	G11
	VCCBRAM-H10	H10
	VCCPINT-G7	G7
	VCCPINT-J7	J7
	VCCPINT-L7	L7
	VCCPINT-N7	N7
	VCCPINT-P8	P8
	VCCPINT-R7	R7
	VCCPLL-G8	G8

1V0 / 1V8 / 1V0 / 1V8 / 1V0 / 1V0
FB1 220 ohms@100MHz 2.0A
C48 10uF 20% 25V — GND
C49 0.47uF 10% 6.3V — GND

VCCO_13

VCCO_13 — C50 47uF 20% 6.3V — C51 4.7uF 10% 6.3V — C52 4.7uF 10% 6.3V — C53 0.47uF 10% 6.3V
C65 0.47uF 10% 6.3V — C66 0.47uF 10% 6.3V — C67 0.47uF 10% 6.3V
GND

Only with XC7Z020

VCCO_34

VCCO_34 — C54 47uF 20% 6.3V — C55 4.7uF 10% 6.3V — C56 4.7uF 10% 6.3V — C57 0.47uF 10% 6.3V
C68 0.47uF 10% 6.3V — C69 0.47uF 10% 6.3V — C70 0.47uF 10% 6.3V
GND

VCCO_35

VCCO_35 — C58 47uF 20% 6.3V — C59 4.7uF 10% 6.3V — C60 4.7uF 10% 6.3V — C61 0.47uF 10% 6.3V
C71 0.47uF 10% 6.3V — C72 0.47uF 10% 6.3V — C73 0.47uF 10% 6.3V
GND

VCCAUX

1V8 — C62 47uF 20% 6.3V — C63 4.7uF 10% 6.3V — C64 0.47uF 10% 6.3V
GND

VCCO_DDR_502

1V2 — C77 100uF 20% 6.3V — C78 4.7uF 10% 6.3V — C79 0.47uF 10% 6.3V
C88 0.47uF 10% 6.3V — C89 0.47uF 10% 6.3V — C90 0.47uF 10% 6.3V
GND

VCCINT

1V0 — C80 100uF 20% 6.3V — C81 100uF 20% 6.3V — C82 100uF 20% 6.3V — C83 4.7uF 10% 6.3V — C84 4.7uF 10% 6.3V
C91 0.47uF 10% 6.3V — C92 0.47uF 10% 6.3V — C93 0.47uF 10% 6.3V — C94 0.47uF 10% 6.3V
GND

VCCPINT

1V0 — C85 100uF 20% 6.3V — C86 4.7uF 10% 6.3V — C87 0.47uF 10% 6.3V
C95 0.47uF 10% 6.3V — C96 0.47uF 10% 6.3V
GND

VCCPAUX

1V8 — C74 47uF 20% 6.3V — C75 4.7uF 10% 6.3V — C76 0.47uF 10% 6.3V
GND

VCCO_MIO0_500

1V8 — C97 100uF 20% 6.3V — C98 4.7uF 10% 6.3V — C99 0.47uF 10% 6.3V
GND

VCCO_MIO0_501

1V8 — C100 100uF 20% 6.3V — C101 4.7uF 10% 6.3V — C102 0.47uF 10% 6.3V
GND

VCCBRAM

1V0 — C103 100uF 20% 6.3V — C104 4.7uF 10% 6.3V — C105 0.47uF 10% 6.3V
GND

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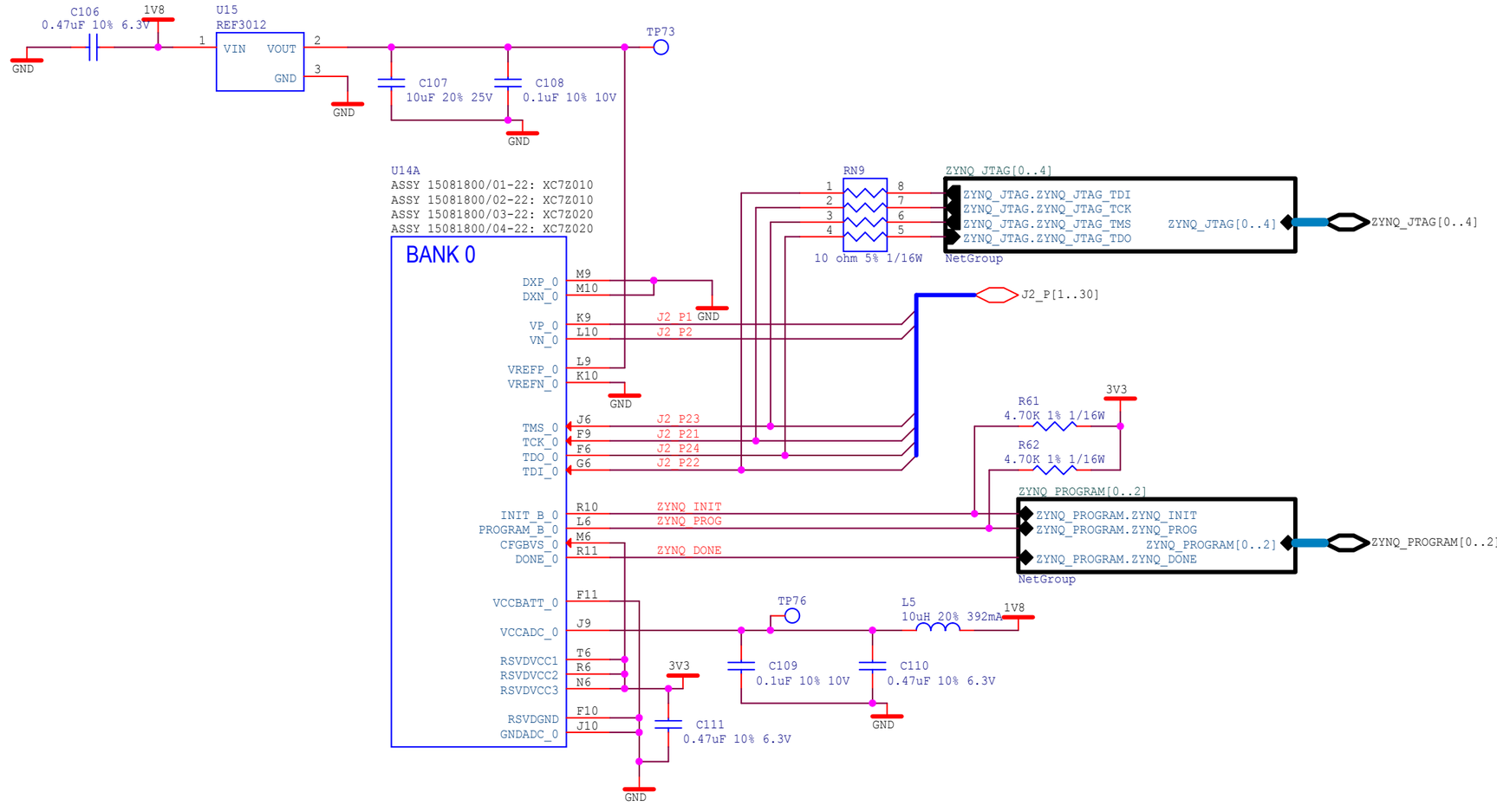
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 20 OF 30



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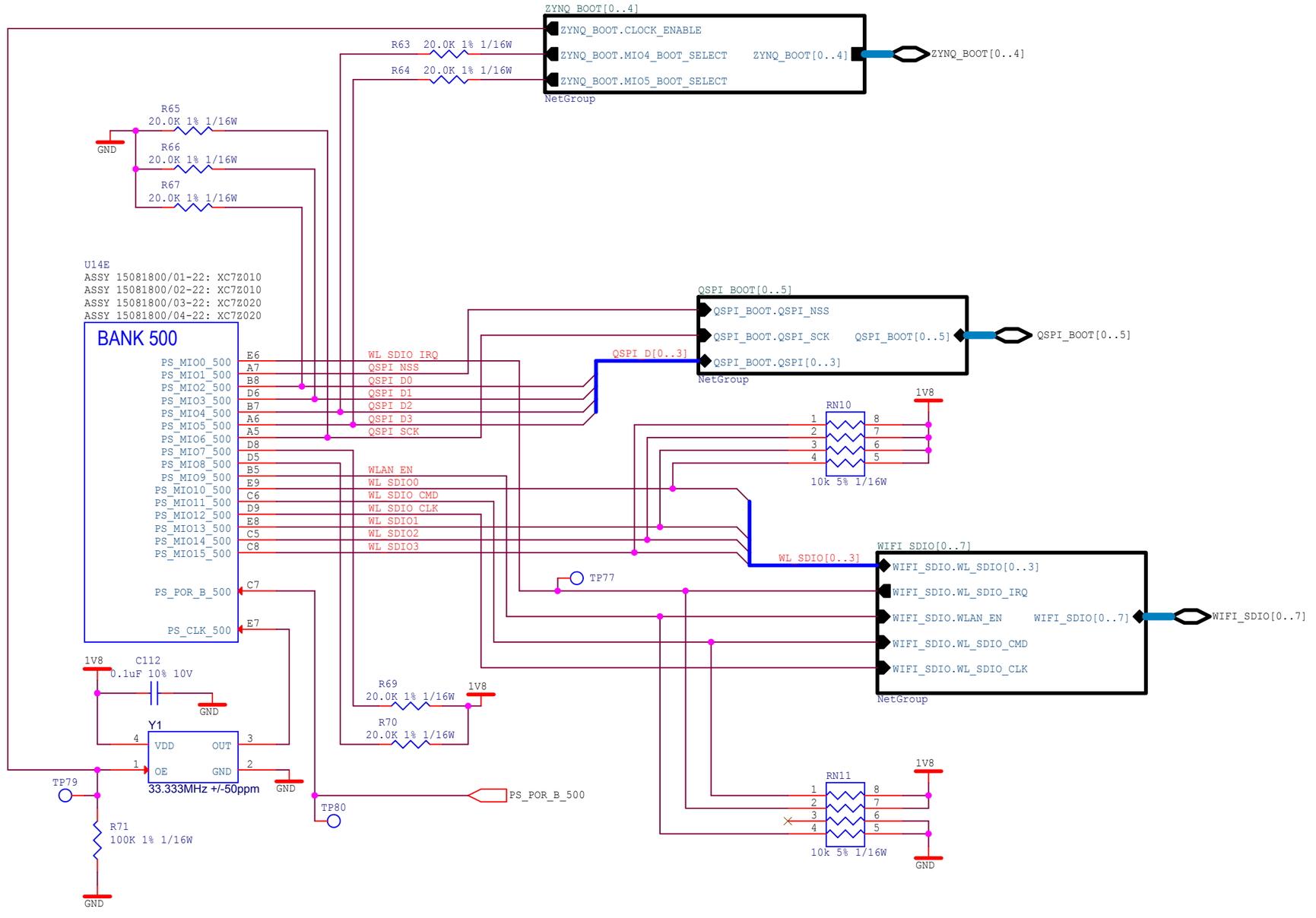
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 21 OF 30



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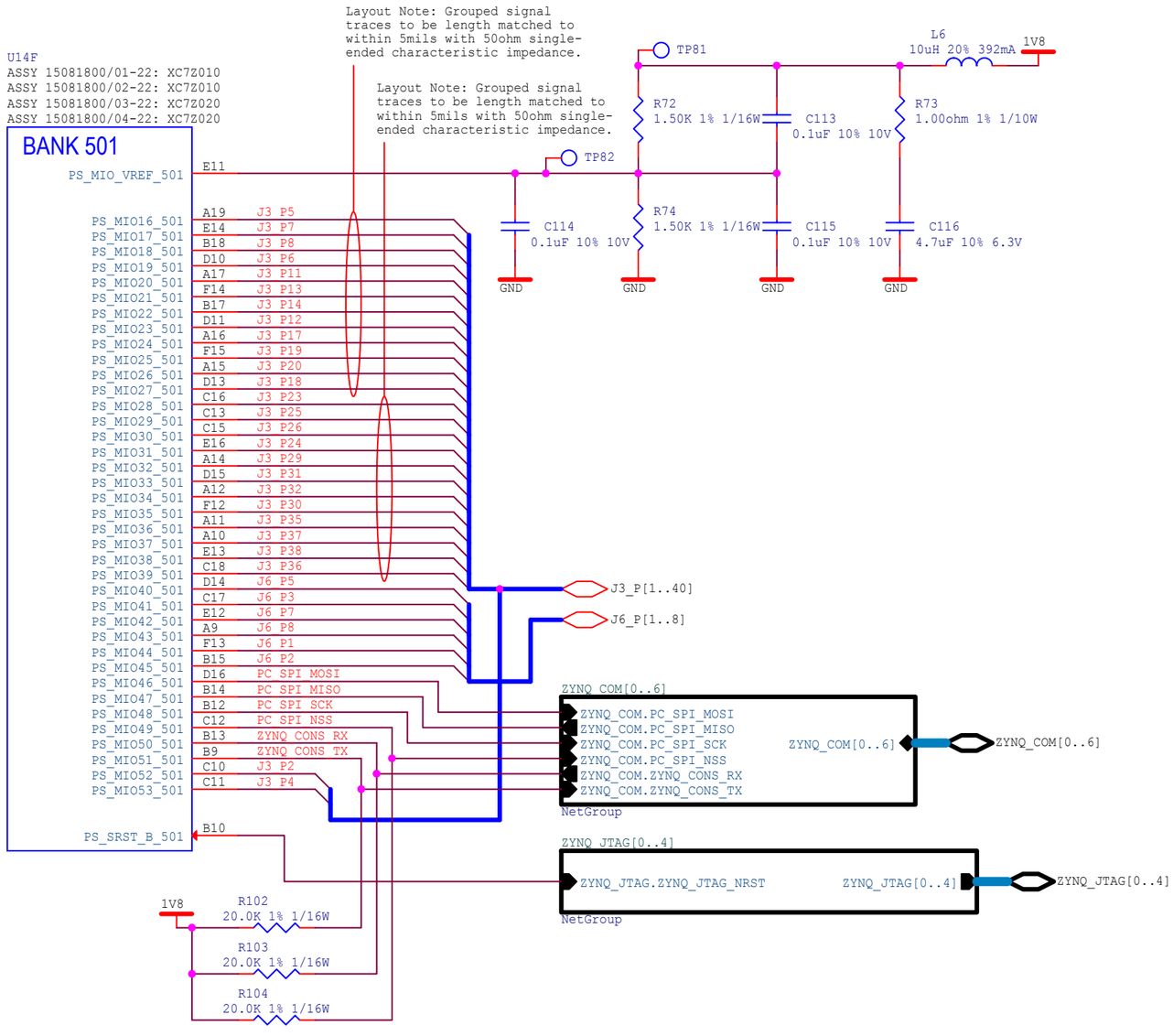
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 22 OF 30



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CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 23 OF 30

U14G
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

BANK 502

PS_DDR_DQ0_502	C3	DQ0
PS_DDR_DQ1_502	B3	DQ1
PS_DDR_DQ2_502	A2	DQ2
PS_DDR_DQ3_502	A4	DQ3
PS_DDR_DQ4_502	D3	DQ4
PS_DDR_DQ5_502	D1	DQ5
PS_DDR_DQ6_502	C1	DQ6
PS_DDR_DQ7_502	E1	DQ7
PS_DDR_DQ8_502	E2	DQ8
PS_DDR_DQ9_502	E3	DQ9
PS_DDR_DQ10_502	G3	DQ10
PS_DDR_DQ11_502	H3	DQ11
PS_DDR_DQ12_502	J3	DQ12
PS_DDR_DQ13_502	H2	DQ13
PS_DDR_DQ14_502	H1	DQ14
PS_DDR_DQ15_502	J1	DQ15
PS_DDR_DQ16_502	P1	DQ16
PS_DDR_DQ17_502	P3	DQ17
PS_DDR_DQ18_502	R3	DQ18
PS_DDR_DQ19_502	R1	DQ19
PS_DDR_DQ20_502	T4	DQ20
PS_DDR_DQ21_502	U4	DQ21
PS_DDR_DQ22_502	U2	DQ22
PS_DDR_DQ23_502	U3	DQ23
PS_DDR_DQ24_502	V1	DQ24
PS_DDR_DQ25_502	Y3	DQ25
PS_DDR_DQ26_502	W1	DQ26
PS_DDR_DQ27_502	Y4	DQ27
PS_DDR_DQ28_502	Y2	DQ28
PS_DDR_DQ29_502	W3	DQ29
PS_DDR_DQ30_502	V2	DQ30
PS_DDR_DQ31_502	V3	DQ31
PS_DDR_A0_502	N2	A0
PS_DDR_A1_502	K2	A1
PS_DDR_A2_502	M3	A2
PS_DDR_A3_502	K3	A3
PS_DDR_A4_502	M4	A4
PS_DDR_A5_502	L1	A5
PS_DDR_A6_502	L4	A6
PS_DDR_A7_502	K4	A7
PS_DDR_A8_502	K1	A8
PS_DDR_A9_502	J4	A9
PS_DDR_A10_502	F5	
PS_DDR_A11_502	G4	
PS_DDR_A12_502	E4	
PS_DDR_A13_502	D4	
PS_DDR_A14_502	F4	
PS_DDR_DQS_P0_502	C2	DQS_P0
PS_DDR_DQS_N0_502	B2	DQS_N0
PS_DDR_DQS_P1_502	G2	DQS_P1
PS_DDR_DQS_N1_502	F2	DQS_N1
PS_DDR_DQS_P2_502	R2	DQS_P2
PS_DDR_DQS_N2_502	T2	DQS_N2
PS_DDR_DQS_P3_502	W5	DQS_P3
PS_DDR_DQS_N3_502	W4	DQS_N3
PS_DDR_CKP_502	L2	CKP
PS_DDR_CKN_502	M2	CKN
PS_DDR_BA0_502	L5	
PS_DDR_BA1_502	R4	
PS_DDR_BA2_502	J5	
PS_DDR_DM0_502	A1	DM0
PS_DDR_DM1_502	F1	DM1
PS_DDR_DM2_502	T1	DM2
PS_DDR_DM3_502	Y1	DM3
PS_DDR_CS_B_502	N1	CS_B
PS_DDR_WE_B_502	M5	
PS_DDR_CAS_B_502	P5	
PS_DDR_RAS_B_502	P4	
PS_DDR_CKE_502	N3	CKE
PS_DDR_ODT_502	N5	
PS_DDR_DRST_B_502	B4	
PS_DDR_VRP_502	H5	
PS_DDR_VRN_502	G5	

R75
40.2 Ohms 1% 1/16W
R76
40.2 Ohms 1% 1/16W
1V2
GND

Layout Note: Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

LPDDR2-SDRAM-IO[0..57]
- LPDDR2-SDRAM-IO.DQ[0..31] ← DQ[0..31]
- LPDDR2-SDRAM-IO.A[0..9] ← A[0..9]
- LPDDR2-SDRAM-IO.DQS_P[0..3] ← DQS_P[0..3]
- LPDDR2-SDRAM-IO.DQS_N[0..3] ← DQS_N[0..3]
- LPDDR2-SDRAM-IO.DM[0..3] ← DM[0..3]
- LPDDR2-SDRAM-IO.CS_B
- LPDDR2-SDRAM-IO.CKE
- LPDDR2-SDRAM-IO.CKP
- LPDDR2-SDRAM-IO.CKN

NetGroup

LPDDR2-SDRAM-IO[0..57] → LPDDR2-SDRAM-IO[0..57]

Layout Note: Route clock on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10-mil spacing from other nets. Length match clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

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CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 24 OF 30

U14D
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

BANK 35

IO_0_35	G14	JA1_P4
IO_L1P_T0_AD0P_35	C20	JA1_P14
IO_L1N_T0_AD0N_35	B20	JA1_P12
IO_L2P_T0_AD8P_35	B19	JA1_P20
IO_L2N_T0_AD8N_35	A20	JA1_P18
IO_L3P_T0_DQS_AD1P_35	E17	JA1_P17
IO_L3N_T0_DQS_AD1N_35	D18	JA1_P19
IO_L4P_T0_35	D19	JA1_P8
IO_L4N_T0_35	D20	JA1_P6
IO_L5P_T0_AD9P_35	E18	JA1_P5
IO_L5N_T0_AD9N_35	E19	JA1_P7
IO_L6P_T0_35	F16	JA1_P11
IO_L6N_T0_VREF_35	F17	JA1_P13
IO_L7P_T1_AD2P_35	M19	JA2_P32
IO_L7N_T1_AD2N_35	M20	JA2_P30
IO_L8P_T1_AD10P_35	M17	JA2_P29
IO_L8N_T1_AD10N_35	M18	JA2_P31
IO_L9P_T1_DQS_AD3P_35	L19	JA2_P23
IO_L9N_T1_DQS_AD3N_35	L20	JA2_P25
IO_L10P_T1_AD11P_35	K19	JA2_P26
IO_L10N_T1_AD11N_35	J19	JA2_P24
IO_L11P_T1_SRCC_35	L16	JA2_P35
IO_L11N_T1_SRCC_35	L17	JA2_P37
IO_L12P_T1_MRCC_35	K17	JA2_P38
IO_L12N_T1_MRCC_35	K18	JA2_P36
IO_L13P_T2_MRCC_35	H16	JA1_P38
IO_L13N_T2_MRCC_35	H17	JA1_P36
IO_L14P_T2_AD4P_SRCC_35	J18	JA1_P35
IO_L14N_T2_AD4N_SRCC_35	H18	JA1_P37
IO_L15P_T2_DQS_AD12P_35	F19	JA1_P23
IO_L15N_T2_DQS_AD12N_35	F20	JA1_P25
IO_L16P_T2_35	G17	JA1_P32
IO_L16N_T2_35	G18	JA1_P30
IO_L17P_T2_AD5P_35	J20	JA1_P29
IO_L17N_T2_AD5N_35	H20	JA1_P31
IO_L18P_T2_AD13P_35	G19	JA1_P26
IO_L18N_T2_AD13N_35	G20	JA1_P24
IO_L19P_T3_35	H15	JA2_P14
IO_L19N_T3_VREF_35	G15	JA2_P12
IO_L20P_T3_AD6P_35	K14	JA2_P20
IO_L20N_T3_AD6N_35	J14	JA2_P18
IO_L21P_T3_DQS_AD14P_35	N15	JA2_P17
IO_L21N_T3_DQS_AD14N_35	N16	JA2_P19
IO_L22P_T3_AD7P_35	L14	JA2_P5
IO_L22N_T3_AD7N_35	L15	JA2_P7
IO_L23P_T3_35	M14	JA2_P11
IO_L23N_T3_35	M15	JA2_P13
IO_L24P_T3_AD15P_35	K16	JA2_P8
IO_L24N_T3_AD15N_35	J16	JA2_P6
IO_25_35	J15	JA2_P4

JA1_P[1..40]

JA2_P[1..40]

U14C
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

BANK 34

IO_0_34	R19	JB2_P4
IO_L1P_T0_34	T11	JB1_P5
IO_L1N_T0_34	T10	JB1_P7
IO_L2P_T0_34	T12	JB1_P8
IO_L2N_T0_34	U12	JB1_P6
IO_L3P_T0_DQS_PUDC_B_34	U13	JB1_P17
IO_L3N_T0_DQS_34	V13	JB1_P19
IO_L4P_T0_34	V12	JB1_P14
IO_L4N_T0_34	W13	JB1_P12
IO_L5P_T0_34	T14	JB1_P20
IO_L5N_T0_34	T15	JB1_P18
IO_L6P_T0_34	P14	JB1_P11
IO_L6N_T0_VREF_34	R14	JB1_P13
IO_L7P_T1_34	Y16	JB1_P26
IO_L7N_T1_34	Y17	JB1_P24
IO_L8P_T1_34	W14	JB1_P29
IO_L8N_T1_34	Y14	JB1_P31
IO_L9P_T1_DQS_34	T16	JB1_P23
IO_L9N_T1_DQS_34	U17	JB1_P25
IO_L10P_T1_34	V15	JB1_P32
IO_L10N_T1_34	W15	JB1_P30
IO_L11P_T1_SRCC_34	U14	JB1_P35
IO_L11N_T1_SRCC_34	U15	JB1_P37
IO_L12P_T1_MRCC_34	U18	JB1_P38
IO_L12N_T1_MRCC_34	U19	JB1_P36
IO_L13P_T2_MRCC_34	N18	JB2_P38
IO_L13N_T2_MRCC_34	P19	JB2_P36
IO_L14P_T2_SRCC_34	N20	JB2_P35
IO_L14N_T2_SRCC_34	P20	JB2_P37
IO_L15P_T2_DQS_34	T20	JB2_P23
IO_L15N_T2_DQS_34	U20	JB2_P25
IO_L16P_T2_34	V20	JB2_P29
IO_L16N_T2_34	W20	JB2_P31
IO_L17P_T2_34	Y18	JB2_P32
IO_L17N_T2_34	Y19	JB2_P30
IO_L18P_T2_34	V16	JB2_P26
IO_L18N_T2_34	W16	JB2_P24
IO_L19P_T3_34	R16	JB2_P14
IO_L19N_T3_VREF_34	R17	JB2_P12
IO_L20P_T3_34	T17	JB2_P11
IO_L20N_T3_34	R18	JB2_P13
IO_L21P_T3_DQS_34	V17	JB2_P17
IO_L21N_T3_DQS_34	V18	JB2_P19
IO_L22P_T3_34	W18	JB2_P20
IO_L22N_T3_34	W19	JB2_P18
IO_L23P_T3_34	N17	JB2_P5
IO_L23N_T3_34	P18	JB2_P7
IO_L24P_T3_34	P15	JB2_P8
IO_L24N_T3_34	P16	JB2_P6
IO_25_34	T19	JB1_P4

JB1_P[1..40]

JB2_P[1..40]

Layout Note: Each grouped pair of signals to have 50ohm single ended and 100ohm differential characteristic impedance.

Layout Note: Grouped signal traces to be length matched to within 10mils.

Layout Note: Grouped signal traces to be length matched to within 10mils.

U14B
ASSY 15081800/01-22: XC7Z010
ASSY 15081800/02-22: XC7Z010
ASSY 15081800/03-22: XC7Z020
ASSY 15081800/04-22: XC7Z020

BANK 13

IO_L6N_T0_VREF_13	V5	JC1_P4
IO_L11P_T1_SRCC_13	U7	JC1_P5
IO_L11N_T1_SRCC_13	V7	JC1_P7
IO_L12P_T1_MRCC_13	T9	JC1_P8
IO_L12N_T1_MRCC_13	U10	JC1_P6
IO_L13P_T2_MRCC_13	Y7	JC1_P38
IO_L13N_T2_MRCC_13	Y6	JC1_P36
IO_L14P_T2_SRCC_13	Y9	JC1_P35
IO_L14N_T2_SRCC_13	Y8	JC1_P37
IO_L15P_T2_DQS_13	V8	JC1_P23
IO_L15N_T2_DQS_13	W8	JC1_P25
IO_L16P_T2_13	W10	JC1_P32
IO_L16N_T2_13	W9	JC1_P30
IO_L17P_T2_13	U9	JC1_P29
IO_L17N_T2_13	U8	JC1_P31
IO_L18P_T2_13	W11	JC1_P26
IO_L18N_T2_13	Y11	JC1_P24
IO_L19P_T3_13	T5	JC1_P11
IO_L19N_T3_VREF_13	U5	JC1_P13
IO_L20P_T3_13	Y12	JC1_P14
IO_L20N_T3_13	Y13	JC1_P12
IO_L21P_T3_DQS_13	V11	JC1_P17
IO_L21N_T3_DQS_13	V10	JC1_P19
IO_L22P_T3_13	V6	JC1_P20
IO_L22N_T3_13	W6	JC1_P18

JC1_P[1..40]

Only available with XC7Z020

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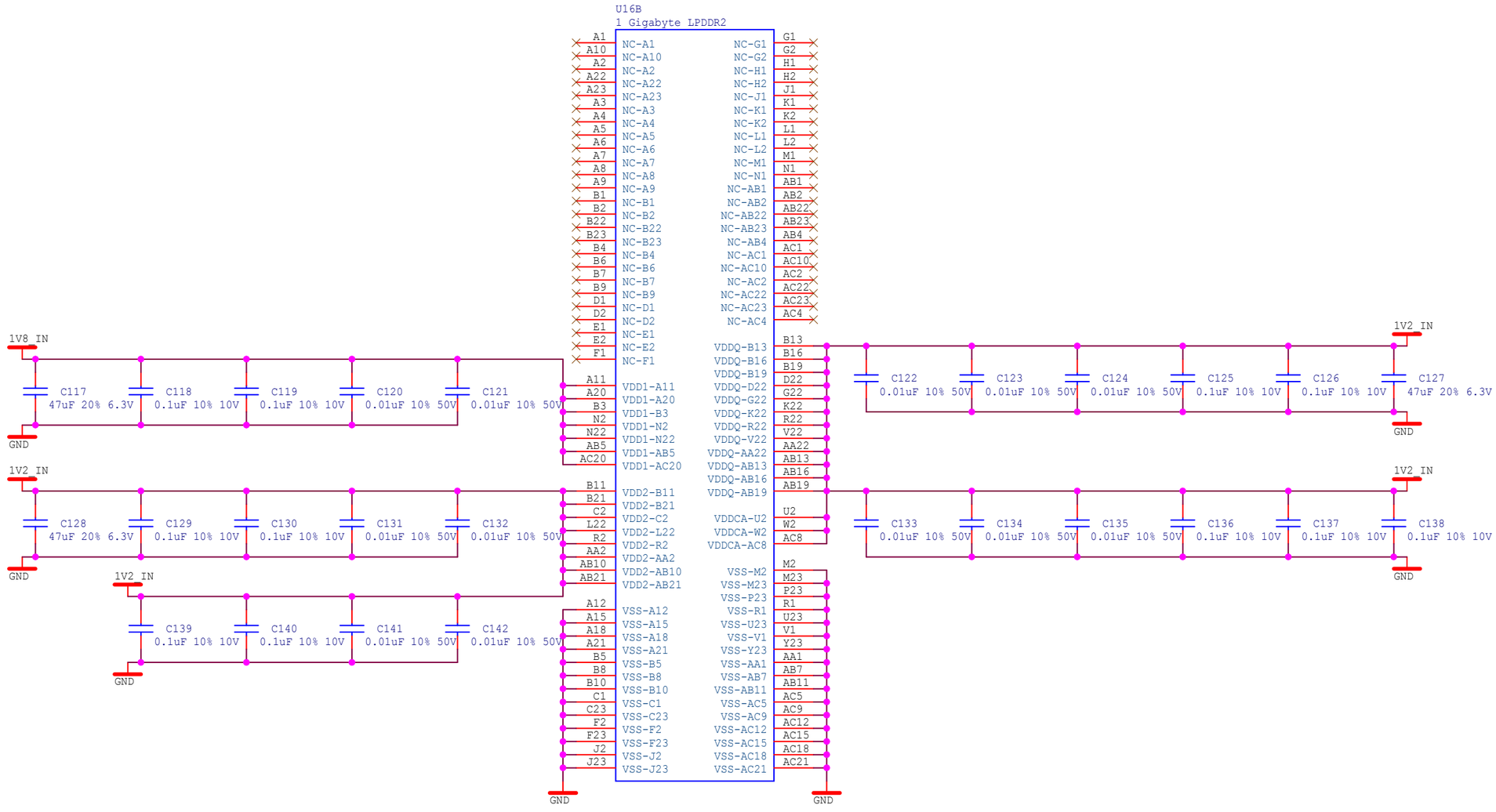
	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X13
DESCRIPTION: Zynq SoC
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 25 OF 30



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	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 26 OF 30

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

Layout Note: Match all signal trace lengths for DQ groups with a max deviation of ±50 mils and route on the same layer.

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO.DQ[0..31]

LPDDR2-SDRAM-IO.DQS_P[0..3]

LPDDR2-SDRAM-IO.DQS_N[0..3]

LPDDR2-SDRAM-IO.DM[0..3]

LPDDR2-SDRAM-IO[0..57]

LPDDR2-SDRAM-IO.CS_B

LPDDR2-SDRAM-IO.CKE

LPDDR2-SDRAM-IO.CKP

LPDDR2-SDRAM-IO.CKN

LPDDR2-SDRAM-IO.A[0..9]

NetGroup

DQ[0..31]

DQS_P[0..3]

DQS_N[0..3]

DM[0..3]

CS_B

CKE

CKP

CKN

A[0..9]

U16A

1 Gigabyte LPDDR2

DQS_P3	B18		DQ31	B12	DQ31
DQS_P2	AB18		DQ30	A13	DQ30
DQS_P1	J22		DQ29	A14	DQ29
DQS_P0	R23		DQ28	B14	DQ28
			DQ27	B15	DQ27
DQS_N3	A19		DQ26	A16	DQ26
DQS_N2	AC19		DQ25	A17	DQ25
DQS_N1	K23		DQ24	B17	DQ24
DQS_N0	P22		DQ23	AC17	DQ23
			DQ22	AB17	DQ22
DM3	B20		DQ21	AC16	DQ21
DM2	AB20		DQ20	AB15	DQ20
DM1	L23		DQ19	AC14	DQ19
DM0	N23		DQ18	AB14	DQ18
			DQ17	AC13	DQ17
CS_B	AB3		DQ16	AB12	DQ16
CKE	AC3		DQ15	C22	DQ15
CKP	Y2		DQ14	D23	DQ14
CKN	Y1		DQ13	E23	DQ13
			DQ12	E22	DQ12
A9	T1		DQ11	F22	DQ11
A8	T2		DQ10	G23	DQ10
A7	U1		DQ9	H23	DQ9
A6	V2		DQ8	H22	DQ8
A5	W1		DQ7	T23	DQ7
A4	AB9		DQ6	T22	DQ6
A3	AB8		DQ5	U22	DQ5
A2	AC7		DQ4	V23	DQ4
A1	AB6		DQ3	W23	DQ3
A0	AC6		DQ2	W22	DQ2
			DQ1	Y22	DQ1
ZQ1	AC11		DQ0	AA23	DQ0
ZQ0	P1				
VREFCA	P2		VREFDQ	M22	

Layout Note: Route clocks on inner layers with outer-layer run lengths held to under 500 mils and maintain a 10 mil spacing from other nets. Length match all clock traces within ±25 mils, with CKP and CKN traces matched within ±10 mils. Do not route CKP/CKN pair and CKE close to address signals.

R77
240 ohm 1% 1/16W

R78
240 ohm 1% 1/16W

R79
4.70K 1% 1/16W

GND

Layout Note: Route address and command signals on a different layer than the data and data mask signals.

L7
10uH 20% 392mA

1V2_IN

TP88

R80
1.00ohm 1% 1/10W

C143
0.1uF 10% 10V

R81
1.50K 1% 1/16W

VREFCA

C145
4.7uF 10% 6.3V

C146
0.1uF 10% 10V

R84
1.50K 1% 1/16W

C147
0.1uF 10% 10V

C148
0.1uF 10% 10V

GND

L8
10uH 20% 392mA

1V2_IN

TP90

R82
1.00ohm 1% 1/10W

C144
0.1uF 10% 10V

R83
1.50K 1% 1/16W

VREFDQ

C149
4.7uF 10% 6.3V

C150
0.1uF 10% 10V

R85
1.50K 1% 1/16W

C151
0.1uF 10% 10V

C152
0.1uF 10% 10V

GND

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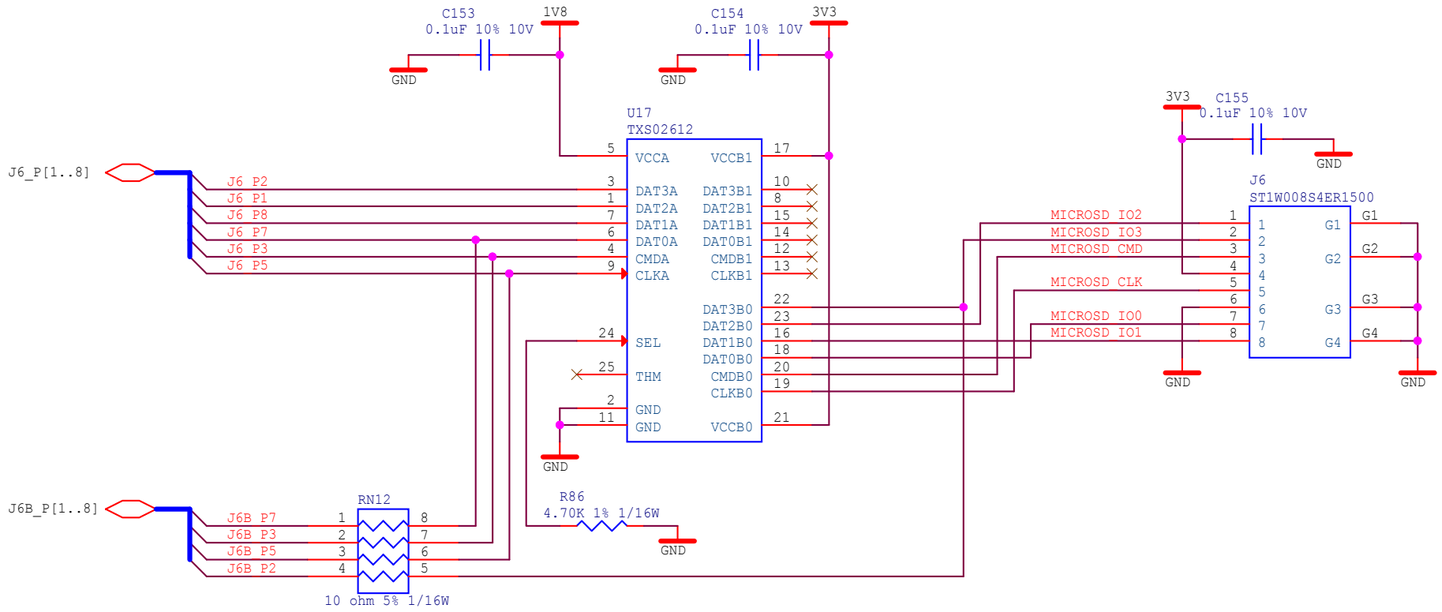
CHECKED BY	J. Weatherbee	11/23/2015
APPROVED BY	J. Weatherbee	11/23/2015

TITLE: snickerdoodle FPGA Module
PATH: /X14
DESCRIPTION: LPDDR2 RAM
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 27 OF 30



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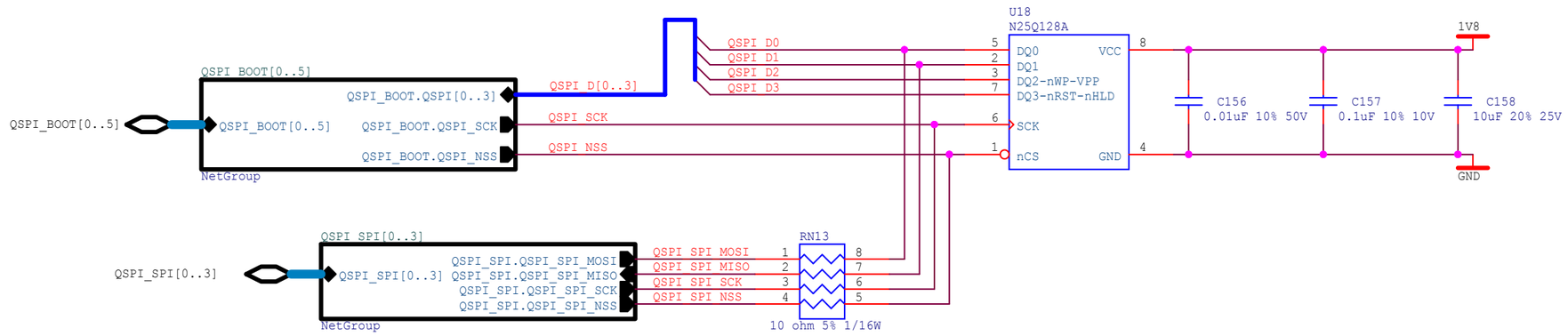
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X15
DESCRIPTION: microSD Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 28 OF 30



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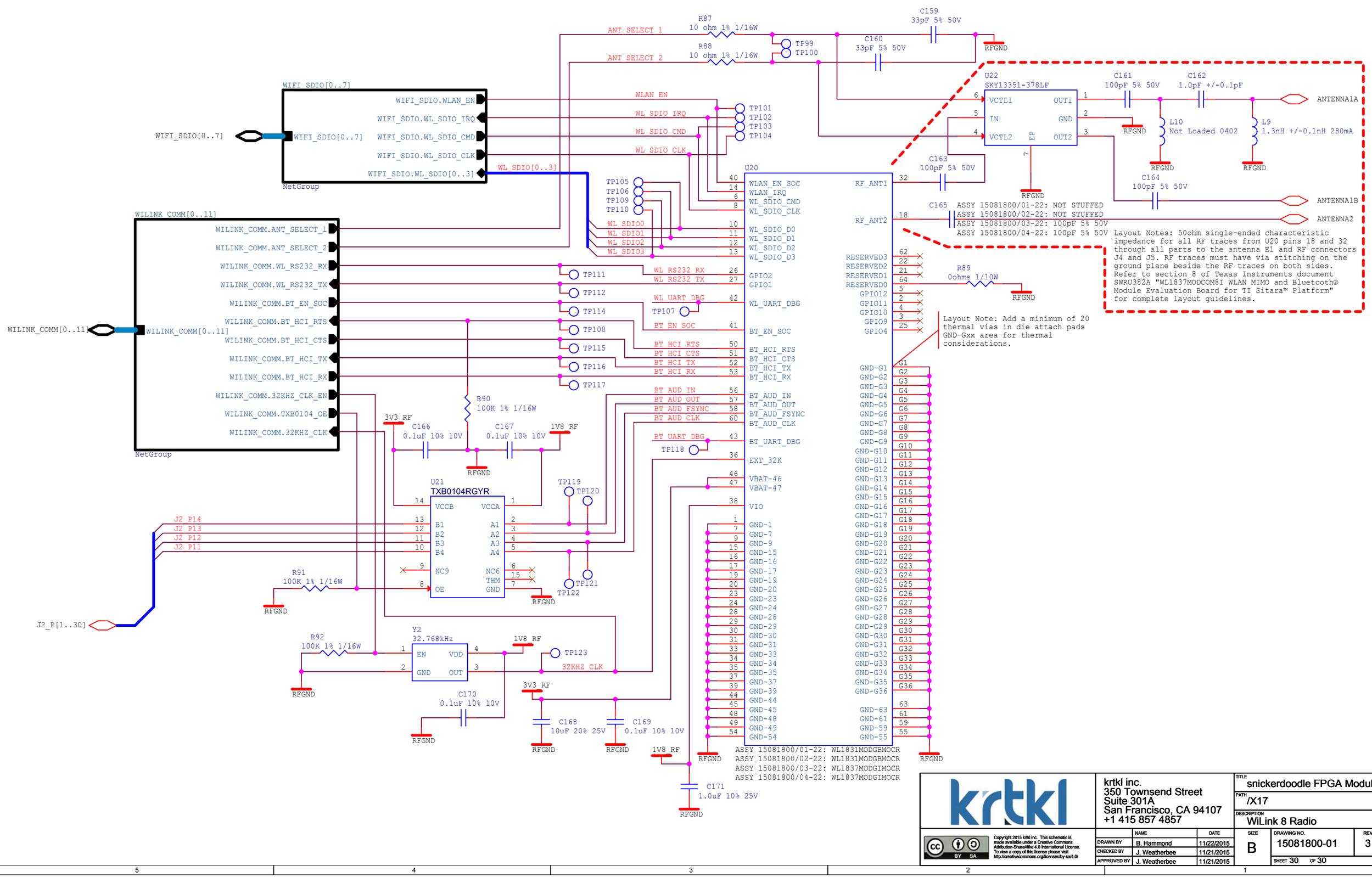
APPROVED BY	J. Weatherbee	11/21/2015

TITLE: snickerdoodle FPGA Module
PATH: /X16
DESCRIPTION: QSPI Flash
SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 29 OF 30



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TITLE: snickerdoodle FPGA Module
PATH: /X17
DESCRIPTION: WiLink 8 Radio

	NAME	DATE
DRAWN BY	B. Hammond	11/22/2015
CHECKED BY	J. Weatherbee	11/21/2015
APPROVED BY	J. Weatherbee	11/21/2015

SIZE: B
DRAWING NO.: 15081800-01
REV: 3
SHEET 30 OF 30

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Net Length (mm)	FPGA Pin	FPGA Signal	JA1		FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JA1_SMB_nINT		
	C19	VCCO_35	3	4	IO_0_35	G14	
104.669	E18	IO_L5P_T0_AD9P_35	5	6	IO_L4N_T0_35	D20	104.650
104.652	E19	IO_L5N_T0_AD9N_35	7	8	IO_L4P_T0_35	D19	104.668
		GND	9	10	GND		
104.658	F16	IO_L6P_T0_35	11	12	IO_L1N_T0_AD0N_35	B20	104.654
104.663	F17	IO_L6N_T0_VREF_35	13	14	IO_L1P_T0_AD0P_35	C20	104.677
		GND	15	16	GND		
104.650	E17	IO_L3P_T0_DQS_AD1P_35	17	18	IO_L2N_T0_AD8N_35	A20	104.672
104.673	D18	IO_L3N_T0_DQS_AD1N_35	19	20	IO_L2P_T0_AD8P_35	B19	104.658
		GND	21	22	GND		
104.063	F19	IO_L15P_T2_DQS_AD12P_35	23	24	IO_L18N_T2_AD13N_35	G20	104.071
104.090	F20	IO_L15N_T2_DQS_AD12N_35	25	26	IO_L18P_T2_AD13P_35	G19	104.083
		GND	27	28	GND		
104.091	J20	IO_L17P_T2_AD5P_35	29	30	IO_L16N_T2_35	G18	104.085
104.066	H20	IO_L17N_T2_AD5N_35	31	32	IO_L16P_T2_35	G17	104.080
		GND	33	34	GND		
104.092	J18	IO_L14P_T2_AD4P_SRCC_35	35	36	IO_L13N_T2_MRCC_35	H17	104.081
104.057	H18	IO_L14N_T2_AD4N_SRCC_35	37	38	IO_L13P_T2_MRCC_35	H16	104.058
		SMB_I2C_SCL0	39	40	SMB_I2C_SDA0		

Net Length (mm)	FPGA Pin	FPGA Signal	JA2		FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JA2_SMB_nINT		
	C19	VCCO_35	3	4	IO_25_35	J15	
58.189	L14	IO_L22P_T3_AD7P_35	5	6	IO_L24N_T3_AD15N_35	J16	58.195
58.203	L15	IO_L22N_T3_AD7N_35	7	8	IO_L24P_T3_AD15P_35	K16	58.191
		GND	9	10	GND		
58.198	M14	IO_L23P_T3_35	11	12	IO_L19N_T3_VREF_35	G15	58.193
58.193	M15	IO_L23N_T3_35	13	14	IO_L19P_T3_35	H15	58.203
		GND	15	16	GND		
58.223	N15	IO_L21P_T3_DQS_AD14P_35	17	18	IO_L20N_T3_AD6N_35	J14	58.213
58.201	N16	IO_L21N_T3_DQS_AD14N_35	19	20	IO_L20P_T3_AD6P_35	K14	58.196
		GND	21	22	GND		
101.835	L19	IO_L9P_T1_DQS_AD3P_35	23	24	IO_L10N_T1_AD11N_35	J19	101.821
101.824	L20	IO_L9N_T1_DQS_AD3N_35	25	26	IO_L10P_T1_AD11P_35	K19	101.819
		GND	27	28	GND		
101.850	M17	IO_L8P_T1_AD10P_35	29	30	IO_L7N_T1_AD2N_35	M20	101.842
101.841	M18	IO_L8N_T1_AD10N_35	31	32	IO_L7P_T1_AD2P_35	M19	101.857
		GND	33	34	GND		
101.841	L16	IO_L11P_T1_SRCC_35	35	36	IO_L12N_T1_MRCC_35	K18	101.782
101.817	L17	IO_L11N_T1_SRCC_35	37	38	IO_L12P_T1_MRCC_35	K17	101.841
		SMB_I2C_SCL1	39	40	SMB_I2C_SDA1		

Net Length (mm)	FPGA Pin	FPGA Signal	JB1		FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JB1_SMB_nINT		
	N19	VCCO_34	3	4	IO_25_34	T19	
101.153	T11	IO_L1P_T0_34	5	6	IO_L2N_T0_34	U12	101.157
101.147	T10	IO_L1N_T0_34	7	8	IO_L2P_T0_34	T12	101.157
		GND	9	10	GND		
101.155	P14	IO_L6P_T0_34	11	12	IO_L4N_T0_34	W13	101.109
101.159	R14	IO_L6N_T0_VREF_34	13	14	IO_L4P_T0_34	V12	101.148
		GND	15	16	GND		
101.146	U13	IO_L3P_T0_DQS_PUDC_B_34	17	18	IO_L5N_T0_34	T15	101.170
101.159	V13	IO_L3N_T0_DQS_34	19	20	IO_L5P_T0_34	T14	101.164
		GND	21	22	GND		
57.498	T16	IO_L9P_T1_DQS_34	23	24	IO_L7N_T1_34	Y17	57.500
57.516	U17	IO_L9N_T1_DQS_34	25	26	IO_L7P_T1_34	Y16	57.510
		GND	27	28	GND		
57.498	W14	IO_L8P_T1_34	29	30	IO_L10N_T1_34	W15	57.499
57.519	Y14	IO_L8N_T1_34	31	32	IO_L10P_T1_34	V15	57.505
		GND	33	34	GND		
57.489	U14	IO_L11P_T1_SRCC_34	35	36	IO_L12N_T1_MRCC_34	U19	57.511
57.516	U15	IO_L11N_T1_SRCC_34	37	38	IO_L12P_T1_MRCC_34	U18	57.486
		SMB_I2C_SCL2	39	40	SMB_I2C_SDA2		

Net Length	FPGA Pin	FPGA Signal	JB2		FPGA Signal	FPGA Pin	
		VIO_OUT (+3.3V)	1	2	JB2_SMB_nINT		
	N19	VCCO_34	3	4	IO_0_34	R19	
66.787	N17	IO_L23P_T3_34	5	6	IO_L24N_T3_34	P16	66.791
66.793	P18	IO_L23N_T3_34	7	8	IO_L24P_T3_34	P15	66.791
		GND	9	10	GND		
66.785	T17	IO_L20P_T3_34	11	12	IO_L19N_T3_VREF_34	R17	66.793
66.789	R18	IO_L20N_T3_34	13	14	IO_L19P_T3_34	R16	66.789
		GND	15	16	GND		
66.779	V17	IO_L21P_T3_DQS_34	17	18	IO_L22N_T3_34	W19	66.800
66.783	V18	IO_L21N_T3_DQS_34	19	20	IO_L22P_T3_34	W18	66.780
		GND	21	22	GND		
39.340	T20	IO_L15P_T2_DQS_34	23	24	IO_L18N_T2_34	W16	39.333
39.358	U20	IO_L15N_T2_DQS_34	25	26	IO_L18P_T2_34	V16	39.352
		GND	27	28	GND		
39.358	V20	IO_L16P_T2_34	29	30	IO_L17N_T2_34	Y19	39.341
39.336	W20	IO_L16N_T2_34	31	32	IO_L17P_T2_34	Y18	39.337
		GND	33	34	GND		
39.344	N20	IO_L14P_T2_SRCC_34	35	36	IO_L13N_T2_MRCC_34	P19	39.350
39.341	P20	IO_L14N_T2_SRCC_34	37	38	IO_L13P_T2_MRCC_34	N18	39.341
		SMB_I2C_SCL3	39	40	SMB_I2C_SDA3		

Net Length (mm)	FPGA Pin	FPGA Signal	JC1		FPGA Signal	FPGA Pin	Net Length (mm)
		VIO_OUT (+3.3V)	1	2	JC1_SMB_nINT		
	T8	VCCO_13	3	4	IO_L6N_T0_VREF_13	V5	
97.389	U7	IO_L11P_T1_SRCC_13	5	6	IO_L12N_T1_MRCC_13	U10	97.442
97.384	V7	IO_L11N_T1_SRCC_13	7	8	IO_L12P_T1_MRCC_13	T9	97.443
		GND	9	10	GND		
97.398	T5	IO_L19P_T3_13	11	12	IO_L20N_T3_13	Y13	97.262
97.394	U5	IO_L19N_T3_VREF_13	13	14	IO_L20P_T3_13	Y12	97.220
		GND	15	16	GND		
97.376	V11	IO_L21P_T3_DQS_13	17	18	IO_L22N_T3_13	W6	97.381
97.393	V10	IO_L21N_T3_DQS_13	19	20	IO_L22P_T3_13	V6	97.397
		GND	21	22	GND		
93.896	V8	IO_L15P_T2_DQS_13	23	24	IO_L18N_T2_13	Y11	93.881
93.862	W8	IO_L15N_T2_DQS_13	25	26	IO_L18P_T2_13	W11	93.865
		GND	27	28	GND		
93.869	U9	IO_L17P_T2_13	29	30	IO_L16N_T2_13	W9	93.866
93.884	U8	IO_L17N_T2_13	31	32	IO_L16P_T2_13	W10	93.875
		GND	33	34	GND		
93.884	Y9	IO_L14P_T2_SRCC_13	35	36	IO_L13N_T2_MRCC_13	Y6	93.877
93.873	Y8	IO_L14N_T2_SRCC_13	37	38	IO_L13P_T2_MRCC_13	Y7	93.872
		SMB_I2C_SCL4	39	40	SMB_I2C_SDA4		

Net Length (mm)	FPGA Pin	FPGA Signal	J3		FPGA Signal	FPGA Pin	Net Length (mm)
	A13	VCCO_MIO1_501 (+1.8V)	1	2	PS_MIO52_501	C10	
		NC	3	4	PS_MIO53_501	C11	
122.875	A19	PS_MIO16_501	5	6	PS_MIO19_501	D10	122.907
122.903	E14	PS_MIO17_501	7	8	PS_MIO18_501	B18	122.888
		GND	9	10	GND		
122.880	A17	PS_MIO20_501	11	12	PS_MIO23_501	D11	122.878
122.895	F14	PS_MIO21_501	13	14	PS_MIO22_501	B17	122.907
		GND	15	16	GND		
122.891	A16	PS_MIO24_501	17	18	PS_MIO27_501	D13	122.883
122.903	F15	PS_MIO25_501	19	20	PS_MIO26_501	A15	122.898
		GND	21	22	GND		
98.732	C16	PS_MIO28_501	23	24	PS_MIO31_501	E16	98.702
98.707	C13	PS_MIO29_501	25	26	PS_MIO30_501	C15	98.731
		GND	27	28	GND		
98.715	A14	PS_MIO32_501	29	30	PS_MIO35_501	F12	98.737
98.735	D15	PS_MIO33_501	31	32	PS_MIO34_501	A12	98.705
		GND	33	34	GND		
98.721	A11	PS_MIO36_501	35	36	PS_MIO39_501	C18	98.711
98.715	A10	PS_MIO37_501	37	38	PS_MIO38_501	E13	98.722
		SMB_I2C_SCL5	39	40	SMB_I2C_SDA5		

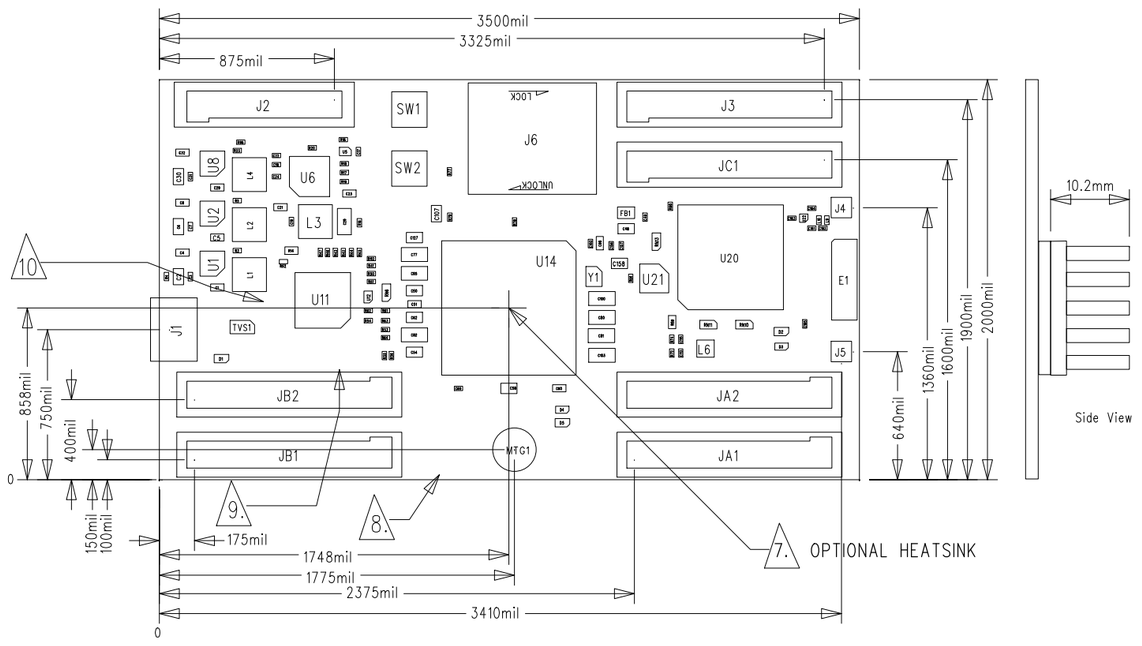
Net Length (mm)	FPGA Pin	FPGA Signal	J2		FPGA Signal	FPGA Pin	Net Length (mm)
	K9	VP_0	1	2	VN_0	L10	
		DAC_OUT1/ADC_IN4	3	4	DAC_OUT2/ADC_IN5		
		GND	5	6	GND		
		SMB_I2C_SCL7	7	8	SMB_I2C_SDA7		
		GND	9	10	GND		
		BT_AUD_CLK	11	12	BT_AUD_FSYNC		
		BT_AUD_OUT	13	14	BT_AUD_IN		
		MCU_SWCLK/PA13	15	16	MCU_SWDIO/PA14		
		MCU_nRST	17	18	MCU_VDDIO2 (+3.3V)		
		Zynq nRST(PS_SRST_B_501)	19	20	GND		
	F9	TCK_0	21	22	TDI_0	G6	
	J6	TMS_0	23	24	TDO_0	F6	
	K6	VCCO_0 (+3.3V)	25	26	PGND		
		GND	27	28	GND		
		VIN (+3.7-17V)	29	30	VIN (+3.7-17V)		

REV	DESCRIPTION	APPD BY	DATE
V1.0			08/01/15
V2.0			01/20/16
V3.0			05/02/16

NOTES: UNLESS OTHERWISE SPECIFIED.

ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION.

1. CONTROLLING DIMENSIONS AND SUPPLIED DATA ARE IN INCHES.
   DIMENSIONS AND TOLERANCES PER ASME Y14.5M.
2. ASSEMBLE IN ACCORDANCE WITH IPC-A-610 CLASS 2.
3. ESD PRECAUTIONS DURING HANDLING AND ASSEMBLY TO BE IN ACCORDANCE WITH EIA JESD 625.
4. MAXIMUM LEAD PROTRUSION ON SECONDARY SIDE TO BE 1.5 MAX.
5. Use water soluble flux for SMT, and no clean flux for secondary solder steps if required
6. Board Cleaning: removal of flux residue is required after first pass SMT, hand solder and rework.
7. OPTIONAL HEATSINK (HS1)
8. SERIAL NUMBER TO BE APPLIED TO RAW PCB FAB PRIOR TO ASSEMBLY, AT LOCATION IDENTIFIED (TOP SIDE).
9. WRITE IN THE ASSEMBLY VARIANT IN THIS BOX ON PRIMARY SIDE SILKSCREEN LAYER
10. WRITE IN THE REVISION IN THIS BOX ON PRIMARY SIDE SILKSCREEN LAYER



THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- INTERPRET DRAWING IAW ASME Y14.100-2000
- DIMENSIONING & TOLERANCING IAW ASME Y14.5-1994
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- DIMENSIONS ARE IN INCHES
- TOLERANCES ARE: ANGLES 1.0
  1 PLACE DECIMAL 0.031
  2 PLACE DECIMAL 0.010
- SURFACE FINISH 63
- REMOVE ALL BURRS AND SHARP EDGES .25 RAD MAX.
- CONCENTRICITY MACHINED DIA: .05 FIM
- MACHINED TOOL MISMATCH .05 MAX.

DRAWING DESCRIPTION
PCB Assembly
Primary Side (TopLayer)

DESIGNER	D. BEANE / J. COX	01AUG2015
ENGINEER	J WEATHERBEE	20JAN2016
CHECK BY	B HAMMOND	20JAN2016
Q. A. BY	J WEATHERBEE	20JAN2016

SECURITY LEVEL
CONFIDENTIAL – STEALTH MODE

DOCUMENT NUMBER 15081800-06 | REV. 3.0

TITLE
PCB, Snickerdoodle

SHEET 1 of 1 | SIZE C | SCALE 1:1

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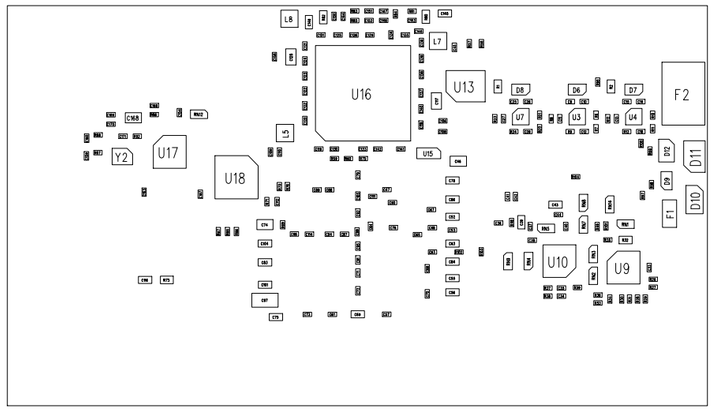
San Francisco, CA
(415) 857-4857
www.krtkl.com

REV | SHT | CORP. NO.

REV	DESCRIPTION	APPD BY	DATE
V1.0			08/01/15
V2.0			01/20/16
V3.0			05/02/16



DRAWING DESCRIPTION: PCB Assembly Secondary Side (BottomLayer)	DOCUMENT NUMBER: 15081800-06	REV.: 3.0
DESIGNER: D. BEANE / J. COX 01AUG2015	TITLE: PCB, Snickerdoodle	
ENGINEER: J WEATHERBEE 20JAN2016		
CHECK BY: B HAMMOND 20JAN2016	SHEET: 2 of 2	SIZE: C
Q. A. BY: J WEATHERBEE 20JAN2016		SCALE: 1:1
SECURITY LEVEL: CONFIDENTIAL – STEALTH MODE	krtkl	350 Townsend Street, Suite 301A San Francisco, CA (415) 857-4857 www.krtkl.com

CORP. NO. SHT REV